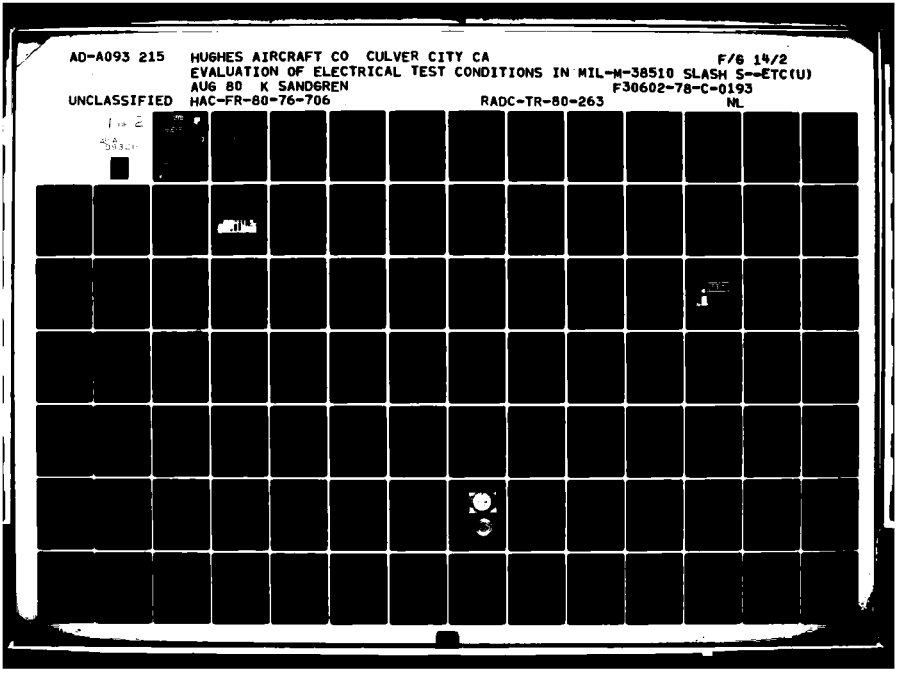
AD-A093 215 HUGHES AIRCRAFT CO CULVER CITY CA F/G 14/2
EVALUATION OF ELECTRICAL TEST CONDITIONS IN MIL-M-38510 SLASH 5--ETC(U)
AUG 80 K SANDGREN F30602-78-C-0193
UNCLASSIFIED HAC-FR-80-76-706 RADC-TR-80-263 NL



LEVEL II

RADC-TR-80-263
Final Technical Report
August 1980

EVALUATION OF ELECTRICAL TEST CONDITIONS IN MIL-M-38510 SLASH SHEETS

Hughes Aircraft Company

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(19) REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER (18) RADC-TR-80-263	2. GOVT ACCESSION NO. AD-A093	3. RECIPIENT'S CATALOG NUMBER 215
4. TITLE (and Subtitle) (6) EVALUATION OF ELECTRICAL TEST CONDITIONS IN MIL-M-38510 SLASH SHEETS		5. TYPE OF REPORT & PERIOD COVERED (9) Final Technical Report August 78 — September 79
	(14) HAC-	6. PERFORMING ORG. REPORT NUMBER FR-80-76-706
7. AUTHOR(s) (10) K. Sandgren		8. CONTRACT OR GRANT NUMBER(s) F30602-78-0193
9. PERFORMING ORGANIZATION NAME AND ADDRESS Hughes Aircraft Company Culver City CA 90203		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62702F 23380157
11. CONTROLLING OFFICE NAME AND ADDRESS Rome Air Development Center (RBRP) Griffiss AFB NY 13441	(11)	12. REPORT DATE August 1980 (12) 13. NUMBER OF PAGES 110 (110)
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Same (15) F30602-78-C-0173		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a. DECLASSIFICATION DOWNGRADING SCHEDULE N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

(16) 2338 (17) 01

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: W. Keith Conroy, Jr. (RBRP)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Microcircuits
Specfication
Automatic Test Equipment
Electrical Testing

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Adequacy of MIL-M-38510 slash sheet requirements for electrical test conditions in an automated test environment were evaluated. Military temperature range commercial devices of 13 types from 6 manufacturers were purchased. Software for testing these devices and for varying the test conditions was written for the Tektronix S-3260 test system. The devices were tested to evaluate the effects of pin-condition settling time, measurement sequence of the same and different D-C parameters, —cont

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172 300

temperature sequence, differently defined temperature ambients, variable measurement conditions, sequence of time measurements, pin-application sequence, and undesignated pin condition ambiguity.

An alternative to current tri-state enable and disable time measurements is proposed; S-3260 "open" and "ground" conditions are characterized; and suggestions for changes in MIL-M-38510 slash sheet specifications and MIL-STD-883 test methods are proposed, both to correct errors and ambiguities and to facilitate the gathering of repeatable data on automated test equipment.

Data obtained showed no sensitivity to measurement or temperature sequence nor to temperature ambient, provided that test times were not excessive. V_{ICP} tests and some low current measurements required allowance for a pin condition settling time because of the test system speed. Some pin condition application sequences yielded incorrect measurements. Undefined terminal conditions of output pins were found to affect I_{OS} and propagation delay time measurements. Truth table test results varied with test frequency and V_{IL} for low-power Schottky devices.

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EVALUATION

The automatic electrical testing of microcircuits has forced a reevaluation of the JAN electrical specification to which devices are procured. Experience has shown that data obtained with automatic test equipment (ATE) very often differs significantly from that obtained on the bench, or even from other ATE. It was the purpose of this study to identify some of those differences and derive new testing procedures that will result in more accurate and repeatable parametric measurements on digital devices.

To this end, hypotheses were tested regarding the effects of test sequence, test condition settling times, and variations in unspecified test conditions. This involved writing computer programs for the test equipment so that several series of measurements could be repeated while carefully changing only one of the questionable parameters at a time, and observing the effects which were manifested in the volumes of data generated. Special analysis programs were therefore written for reducing this data. Also, the existing tri-state time measurement technique in one of the specs was found inadequate and a new, more accurate and more meaningful method was proposed.

The problem of how to define the ambient temperature of a device was addressed by performing experiments with different heating and cooling techniques. This data, combined with the application of thermodynamic principles involved in determining T_J and T_A, led to some proposed changes to MIL-STD-883, "Test Methods and Procedures for Microelectronics." This work required a great deal of insight into the operation of the ATE itself, such as knowing how the

equipment makes a measurement when the appropriate statement is encountered in the software, and understanding the parasitic elements of the test equipment's electrical measurement paths and nodes.

As a result of this work, improvements can be made not only to MIL-STD-883, but also MIL-M-38510, "Military Specification Microcircuits General Specification For," and the specific slash sheets reviewed in this effort. This impacts both the quality of the part procured to the spec, as well as the repeatability of data taken on different ATE systems when programmed to test to the same electrical spec.

This effort, however, covers only small and medium scale digital microelectronics. In order to fill the need for a detailed inspection and verification of JAN electrical specs, this work must be extended to cover linear and large scale complex microcircuits as well. This will contribute significantly to assuring the reliability of parts procured to the JAN spec system, which is one of the most important aspects of the R5B TPO thrust in Solid State Device Reliability.

W. Keith Conroy Jr.

W. KEITH CONROY, JR.
Project Engineer

1. INTRODUCTION

This final report summarizes the results of a study completed by the Technology Support Division of Hughes Aircraft Company under Rome Air Development Center, Contract No. F30602-78-C-0193. The title of this study is "Evaluation of Electrical Test Conditions in MIL-M-38510 Slash Sheets." The test and evaluation period was from August 1978 to September 1979.

Integrated circuit test facilities typically use computer-controlled automatic test systems which perform hundreds of voltage, current, and time measurements in a few seconds. However, the systems in use have varying capabilities. Also, test engineers in different facilities do not always use the same test techniques. These differences have occasionally resulted in correlation problems between facilities. Factors that have caused problems include the following:

1. Undefined pin conditions, such as those resulting from failure to define the input or load for pins not included in the immediate test. (These pins are assumed to have no effect on test results.)
2. The sequence for the application and removal of bias supplies.
3. Such variables as test sequence, stimulus rise time, post-measurement settling time, chip heating as a function of test duration, and chip temperature control methods.

Many of these variables, which can potentially affect test results, are encountered only in the use of automatic test equipment (ATE). Thus, test specifications prepared before the widespread use of computer-controlled automatic test systems often fail to define some of these variables. Some existing MIL-M-38510 microcircuit specifications and MIL-STD-883 test methods fall into this category.

The principal objectives of this program have been to review existing MIL-M-38510 slash sheet electrical test conditions and evaluate the effects on parameter measurements of variations in test conditions where allowed in the specification. Such variables as undesignated pin options, measurement sequence, temperature environment, test set-up time, test recovery time, and temperature sequence were evaluated as well as the adequacy of

definitions of "open" and "ground" pin conditions. The specifications were also reviewed for errors and superfluous tests. These factors were evaluated for an automated testing environment where timing, test sequence, and other factors become important parts of the specification.

All of the tests were performed at the Hughes Aircraft Culver City facility on one of three Tektronix S-3260 automated IC test systems, illustrated in Figure 1. All test personnel contributing to the study are part of Hughes Technology Support Division, Components Laboratory.

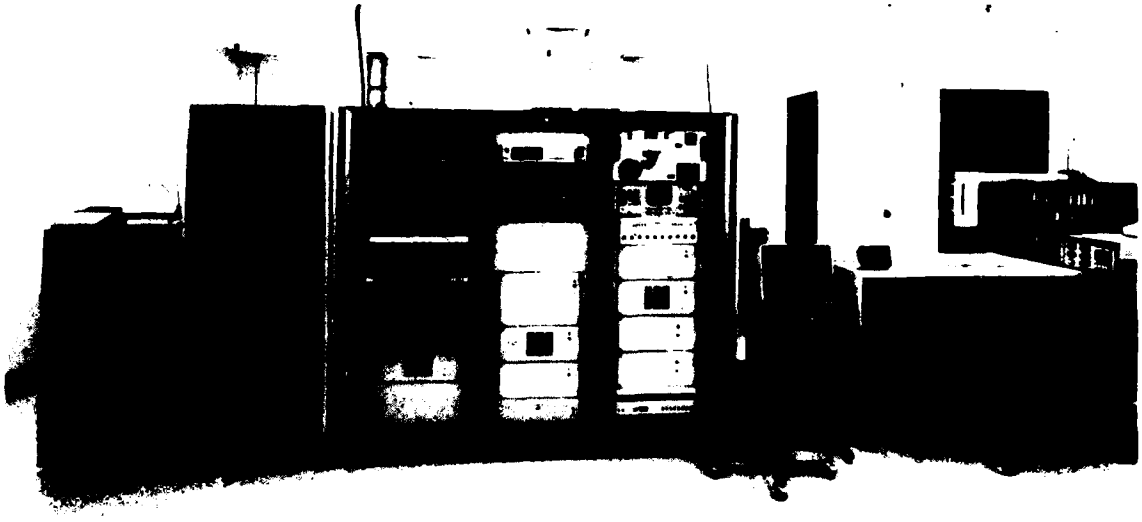


Figure 1. S-3260 Microelectronic test system

2. DESCRIPTION OF STUDY

The scope of this study includes the completion of 15 tasks as outlined in Table 1. Tasks 1, 2, and 3 are interrelated and required completion before any of the remaining 12 tasks or studies could be initiated.

TEST PLAN

Task 1 required parts selection and procurement from vendors listed on the qualified parts list (QPL). Within the time frame of this study, 6 vendors were able to supply 15 samples of each device type required. In all, 13 device types, representing each of the major TTL device families and the CMOS devices currently used in military hardware, were tested during the course of this study. These devices include gates, flip-flops, and a shift register from each family. As Table 2 shows, 26 sets of 15 vendor parts were received for testing, for a total of 390 purchased parts.

All 390 purchased parts were submitted to initial electrical measurements at the three temperatures of -55°C, +25°C, and +125°C. Then 10 samples from each group of 15 parts were selected as test samples and used in the test method evaluation studies. Two samples from each group were retained as control samples and were not subjected to evaluation studies. The remaining three samples from each group were set aside for contingencies.

The 10 test samples from each of the 26 vendor sets formed the 260-sample test group for the remainder of the study. These parts were subjected to a series of tests designed to measure the effectiveness and adequacy of the applicable military specification in an automated test environment. The tests varied settling time, measurement sequence, temperature sequence, and different temperature ambients, and measured their effects.

TABLE 1. TASK OR STUDY DESCRIPTION TABLE

Task No.	Test Samples	Description of Task or Investigation	Temperature (°C)
1	15 per vendor	Parts Selection and Procurement	NA
2	NA	Initial Programming Effort	NA
3	390	Initial Electrical Tests Required by Slash Sheets	25, -55, +125
4	260	Effects of Pin Condition Settling Time	25
5	260	Effects of Measurement Sequence of Different Parameters	25
6	260	Effects of Temperature Sequence	25, -55, +125
7	260	Effects of Differently Defined Ambients	25, -55, +125
8	260	Effects of Variable Measurement Conditions	25, -55, +125
9	260	Effects of Sequence in Time Measurements	25
10	260	Effects of Measurement Sequence of the Same Parameter	25
11	260	Effects of Pin Application Sequence	25
12	260	Effects of Undesignated Pin Ambiguity	25, -55, +125
13	52	Effectiveness of Test Measurement	25
14	52	Defining Open and Ground	25
15	260	Effects of Measurement Times and Time between Measurements	25, -55, +125

TABLE 2. DEVICE TYPES AND SUPPLIERS

Part No.	RCA	SIG	NSC	FSC	TI	MOT
5400		X	X	X	X	X
54H00		X		X	X	X
54S00		X				
54LS00		X	X	X		
4011A	X		X			
5474				X		
54H74		X				
54S74		X				
54LS74					X	X
4013A	X		X			
54164		X				
54LS295					X	
4015A	X		X			

Note: RCA - RCA Corp, Solid State Div
SIG - Signetics Corp
NSC - National Semiconductor
FSC - Fairchild
TI - Texas Instruments
MOT - Motorola Semiconductor

PLAN FOR INVESTIGATING SEQUENCE SENSITIVITIES

The investigation of sequence related sensitivities requires a large number of tests. Since the majority of tasks included in this study involve some sort of sequence investigation, the approach used is as follows:

1. Tests were run (or pins were tested) in groups of N, so that there would be no difference in program flow for different sequences.
2. Each test (or pin) appeared at least once in each position of a group (i.e., 1st, 2nd, 3rd, ... Nth).
3. Each test (or pin) was followed and preceded by each of the other tests (or pins) at least once.
4. A minimum number of tests were performed to minimize both data and test run times.
5. The sequences were generated automatically within the test program to facilitate data logging and reduction and to minimize programming errors.

An algorithm was developed which meets these sequencing requirements. It can be shown that for any even N tests performed in sequence, the minimum number of test runs is N, for a total of N^2 tests. For odd numbers the number of test runs becomes N+1, for a total of $(N + 1)^2$ tests. Therefore, for a sequence of ten tests, the minimum matrix of tests would be as shown in Table 3, where each column represents a test run of ten items.

TABLE 3. TEST MATRIX FOR SEQUENCE OF TEN MEASUREMENTS

Sequence Number									
1	2	3	4	5	6	7	8	9	10
1	3	5	7	9	10	8	6	4	2
2	1	3	5	7	9	10	8	6	4
3	5	7	9	10	8	6	4	2	1
4	2	1	3	5	7	9	10	8	6
5	7	9	10	8	6	4	2	1	3
6	4	2	1	3	5	7	9	10	8
7	9	10	8	6	4	2	1	3	5
8	6	4	2	1	3	5	7	9	10
9	10	8	6	4	2	1	3	5	7
10	8	6	4	2	1	3	5	7	9

In order to use the same algorithm for both even and odd numbers, it becomes necessary to generate the matrix for the next higher even number and substitute the highest odd number for the highest even number. Thus, a matrix for the number 9 would be exactly the same as the Table 3 example except that all 10s would be replaced with 9s. This substitution generates some redundancies, but in order to conform to requirement 1, that all tests be run in groups of N, the step is unavoidable.

3. INITIAL PROGRAMMING AND TEST

In order to manipulate test sequences, as was required throughout this investigation, very flexible test software is necessary. Although programs were available in-house for 11 of the 13 device types used, the existing software for 8 of these was found not to be sufficiently flexible. Therefore, new programs were written for these 8 as well as for the 2 with no program, and extensive modifications were made to the remaining 3 programs. Because of test equipment limitations, some tests called out in the MIL-M-38510 slash sheets were modified or eliminated, as indicated in Table 4. The initial programs were written with minimized test set-up times. Minimum time between measurements was sought, but the constraints of the required measurement flexibility forced some compromises. A special minimum-time-between-measurements program for the 5400 (/00104) was written using "brute-force" techniques limiting the use of variables, loops, call statements, and conditional statements. Then the results were compared to the corresponding program used in this investigation. No significant measurement differences were encountered (see Table 5).

Fifteen devices per qualified vendor per slash sheet were purchased and tested to the conditions of the appropriate specification (as excepted in Table 4). Table 6 furnishes a summary of the initial test results. A zero denotes no failed devices for the parameter tested. As the data reveals, seven device types remained within limits throughout the testing. In addition, three CMOS device types remained within limits except that V_{ICP} tests required a delay for pin condition settling. Only three device types failed any of the parametric tests, and these failures were marginal. These parts were carefully included in the groups of ten parts per vendor per slash sheet so that changes in test method which might permit marginally failing parts to pass or marginally passing parts to fail might be more easily detected.

TABLE 4. EXCEPTIONS TO MIL-M-38510 TEST CONDITIONS

	Test Type	Problem Preventing Compliance	Resolution	Slash Sheets Affected
1.	Maximum Frequency Test	Machine clock rate capability is only 20.48 MHz. Faster requirements could not be met.	Where slash sheet requires higher clock rates, F max calculated from propagation delays, set up, hold, and minimum pulse width times.	/00903, rev C /00203, rev B /07101, rev A
2.	Propagation Delay Times	Slash sheet rise, fall time requirements could not be met without modifying test equipment.	Existing system rise, fall times of 4 ns were used.	/07001 /07101, rev A /05001, rev B /05101, rev B
3.	Propagation Delay Times	Slash sheet requires a pulse width of 5 ns on an input. System minimum is 8 ns.	8 ns used in place of 5 ns.	/07101, rev A
4.	Input Capacitance Test	System does not have capability to measure input capacitance directly.	Test not done.	/05001, rev B /05101, rev B /05703, rev B
5.	All Tests	54LS295B not available in time for study.	54LS295A used and input, output currents modified to limitations of this device type.	/30606, rev A

TABLE 5. DATA COMPARISON BETWEEN SPECIAL PROGRAM AND INITIAL PROGRAM

Parameter (5400-Type Device at 25°C)	Special Program (Minimum Time between Measurements) Mean	Special Program (Minimum Time between Measurements) Standard Deviation	Initial Program (Baseline) Mean	Initial Program (Baseline) Standard Deviation	Units
t_{PHL}	9.888	0.787	9.885	0.784	ns
t_{PLH}	9.291	0.748	9.296	0.753	ns
V_{OH}	2.802	0.202	2.806	0.201	V
V_{OL}	237.1	23.9	234.2	24.0	mV
I_{OS}	-36.10	5.68	-36.08	5.65	mA
I_{IL}	-1.067	0.074	-1.067	0.074	mA
I_{IH_1}	4.923	3.17	4.980	3.14	μA
I_{IH_2}	6.587	3.81	6.600	3.84	μA
I_{CCH}	4.732	0.370	4.735	0.372	mA
I_{CCL}	15.22	1.53	15.21	1.52	mA
V_{IC}	-1.100	0.230	-1.095	0.231	V

TABLE 6. SUMMARY OF INITIAL TEST RESULTS

Device Type and Number of Type	Temperature	Test Lot	AC Parameters t_{PLH}	t_{PHL}	Other	DC Parameters Output V_{OH}	V_{OL}	I_{OS}	Input V_{IC}	I_{IH}	I_{IL}	Other I_{CC}/I_{SS}
	-55	[illegible]		[illegible]	[illegible]	0		1[5]	N/A[5]			
5400	25				[illegible]	[illegible]	0		[illegible][2]			1
[illegible]	125	[illegible]				[illegible]	[illegible]	0	N/A		[illegible]	[illegible]
	-55	[illegible]		[illegible]		0	[illegible]	[illegible]	N/A	[illegible]		
54H00	25	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]			
60	125	[illegible]			[illegible]	[illegible]	[illegible]	[illegible]	N/A	[illegible]		
	-55		[illegible]		[illegible]		[illegible]	[illegible]	N/A	[illegible]	[illegible]	[illegible]
54S00	25	[illegible]			[illegible]		[illegible]	[illegible]	[illegible]			[illegible]
15	125	[illegible]	[illegible]			[illegible]	[illegible]	[illegible]	N/A			
	-55	[illegible]		[illegible]			[illegible]	[illegible]	N/A			
54LS00	25	[illegible]	5	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]			
45	125	0		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	N/A	[illegible]	[illegible]	
	-55	0	[illegible]	0	[illegible]	[illegible]	[illegible]	N/A				
4011	25	0	[illegible]	[illegible]	0	0	[illegible]	N/A	4			[illegible]
30	125	0	0	[illegible]	0	0	0	N/A				
	-55	0	0	0	0	[illegible]	0	[illegible]	N/A	[illegible]		[illegible]
5474	25	0	0	0	0	0	0	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
15	125	0	0	0	0	0	0	[illegible]	N/A			
	-55	0	0	0	0	[illegible]	0		N/A			
54H74	25	0	0	0	0	0	0	[illegible]	0	[illegible]	[illegible]	
15	125	0	0	0	0	0	[illegible]		N/A			
	-55	[illegible]	0	0	0	0	0	[illegible]			[illegible]	
54S74	25	0	0	0	0	0	0	0	[illegible]			[illegible]
15	125	0	0	0	0	0	[illegible]	0		[illegible]		[illegible]
	-55	0	0	0	0	0	[illegible]	0	N/A	0	0	0
54LS74	25	0	0	0	0	0	[illegible]	0	0	[illegible]	0	0
30	125	0	[illegible]	0	0	0	0	0	N/A	[illegible]	0	0
	-55	0	0	0	0	0	0	N/A			0	[illegible]
4013	25	0	0	0	0	0	0	N/A	4	[illegible]	[illegible]	0
30	125	0	0	0	0	0	0	N/A		[illegible]	0	0
	-55	[illegible]	[illegible]	0	0	0	0	0	N/A	[illegible]	0	[illegible]
54164	25	0	0	0	0	0	0	0	0	[illegible]	0	
15	125	0	0	[illegible]	0	0	0	0	N/A	0	0	0
	-55	0	0	0	0	0	0	0	N/A	0	[illegible]	[illegible]
54LS164	25	0	0	0	0	0	0	0	0	[illegible]	0	[illegible]
15	125	1[6]	0	0	0	[illegible]	0	0	N/A	0	0	[illegible]
	-55	0	0	0	0	0	0	N/A		[illegible]	0	[illegible]
401[illegible]	25	0	0	0	0	0	0	N/A	4	[illegible]	[illegible]	[illegible]
30	125	0	0	0	0	0	0	N/A		0	0	

1 N/A = Not applicable.

2 [illegible] Motorola yielded a typical V_{IC} value of [illegible] Volts. Specification limit is [illegible] Volts.

3 [illegible] I_{OS} at -55°C. Specification limits are [illegible] I_{OS} [illegible] mA. Measured [illegible] are [illegible] I_{OS} [illegible] 21 mA.

4 [illegible] of repetition without insertion of a delay to allow for [illegible] settling.

5 Less than 10 percent out of specification.

6 Failures due to running test with V_{IL} [illegible] 0.7V and a PRR of 1 MHz.

4. EFFECTS OF PIN CONDITION SETTLING TIME

TEST DESCRIPTION

Pin condition settling time is the time between establishment of measurement conditions and the time at which a measurement is made. In the case of I_{IH_1} on 5400 devices, for example, all pin conditions except for those on the pin to be measured were set up. V_{CC} was forced with the appropriate voltage (5.5V) and the other inputs were grounded. The specified voltage (2.4V) was forced at the input pin at some time t_0. The measurement was then made at some later time t_1. The pin condition settling time is $t_1 - t_0$. The purpose of this study was to determine the effects of different pin condition settling times.

The baseline programs developed for the initial test were modified by inserting a variable delay between measurement condition setup and actual measurement (Figure 2). The S-3260 test systems used have a 1 ms minimum pin condition settling time for all measurements except the lowest range (100 ma) of current measurement. This system value is limited by

```
 1.0100 *  SN5400
 1.0200 *  QUADRUPLE 2 INPUT POSITIVE NAND GATE
    :
    :
 4.9000    ARRAY DLY(8)
 4.9100    PRESET DLY=0,1M,2M,4M,9M,99M,999M,9.999
    :
    :
 8.4000    LOOP 190.13 N=1,8
    :
    :
44.0100 *  IIH1
44.0200 *
44.0300    VS4=5.5V,200MA
44.0400    LOOP 44.16 X=1,8
44.0500    I.DRIVE=0.0V ON INS
44.0600    DISCONNECT INPUT FROM DRIVER ON INS(X)
44.0700    SETUP TO MEASURE CURRENT ON INS(X) FROM VS4=2.4V AT 100A
44.0710    WAIT DLY(N)*1S
44.0800    IIH1(X)=CURRENT
44.0900    UNSET TO MEASURE CURRENT ON INS(X) FROM VS4
44.1000    IF(IIH1(X) LT 100A)44.14
44.1100    SETUP TO MEASURE CURRENT ON INS(X) FROM VS4=2.4V AT 100UA
44.1110    WAIT DLY(N)*1S
44.1200    IIH1(X)=CURRENT
44.1300    UNSET TO MEASURE CURRENT ON INS(X) FROM VS4
44.1400    CONNECT INPUT TO DRIVER ON INS(X)
44.1600    CONTINUE
    :
    :
190.1200   CONTINUE
190.1300   CONTINUE
190.1400   SN=SN+1
```

Figure 2. Example of the insertion of a variable delay from the program used for the 5400 devices

the time that it takes for switching reeds and the measurement system to settle. This delay is part of the system hardware-software interface not subject to reduction by the test engineer. Delays of 0 ms, 1 ms, 2 ms, 4 ms, 9 ms, 99 ms, 999 ms, and 9.999 s were added to the inherent 1 ms delay of the test system to give measurement delays of 1 ms, 2 ms, 3 ms, 5 ms, 10 ms, 100 ms, 1 second, and 10 seconds. Ten parts per vendor per slash sheet were tested at each delay value, except 1 second and 10 seconds. Because of the long test times required at 1 and 10 seconds per measurement, only two parts per vendor per slash sheet were tested for these conditions. Also, input current measurements on CMOS devices were not tested. Because of delays inherent in the MC-1 low current measurement option on our S-3260 (delays which can reach 3 seconds per measurement), adding extra milliseconds was deemed superfluous and costly in terms of test time.

In evaluating the data for low current measurements (typically I_{IH_1} for Schottky or low-power Schottky parts), wide measurement swings were observed (see Figure 3). The S-3260 tester appears to be responsible for

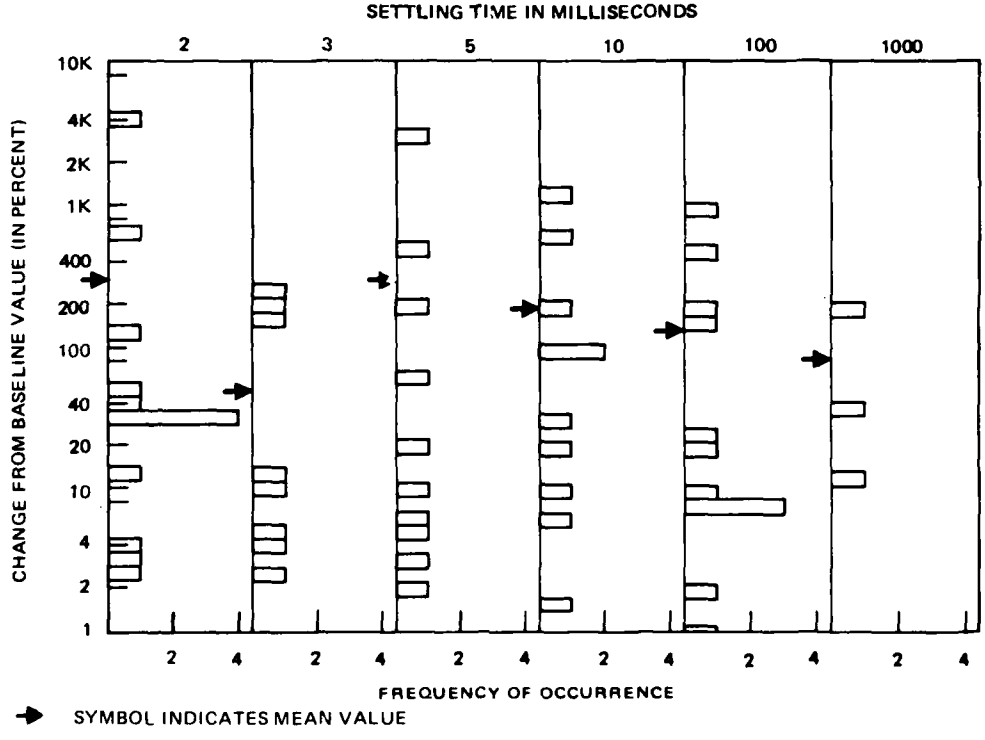


Figure 3. Large variations in I_{CEX} readings of 54S74 devices at 25°C

this inconsistent data. Repeatedly measuring current on a fixture with no device in the socket and plotting the current measured versus the delay in the measurement shows a noise with a frequency of between 120 and 150 Hz and an amplitude that depends on the current range and the particular S-3260 system used (see Figure 4). The amplitude was as high as 14.5 nA peak-to-peak on the 1 μA range of one system, and as high as 9 nA peak-to-peak on the 100 nA range, whereas it was necessary to measure leakage currents of 2 nA. Fortunately, one system had much smaller variations (2 nA peak-to-peak). Using this system, with 5 nA as the significance guideline on the 100 nA range, the remainder of the data was taken without further difficulty.

RESULTS AND CONCLUSIONS

The bulk of the data showed no dependence on pin condition settling time. Table 7 summarizes the data from the 5400-type devices where the mean values changed by less than 2 percent in all cases. It would be expected that measurements requiring significant power dissipation would be dependent on the length of time a forcing voltage or current was applied. While such

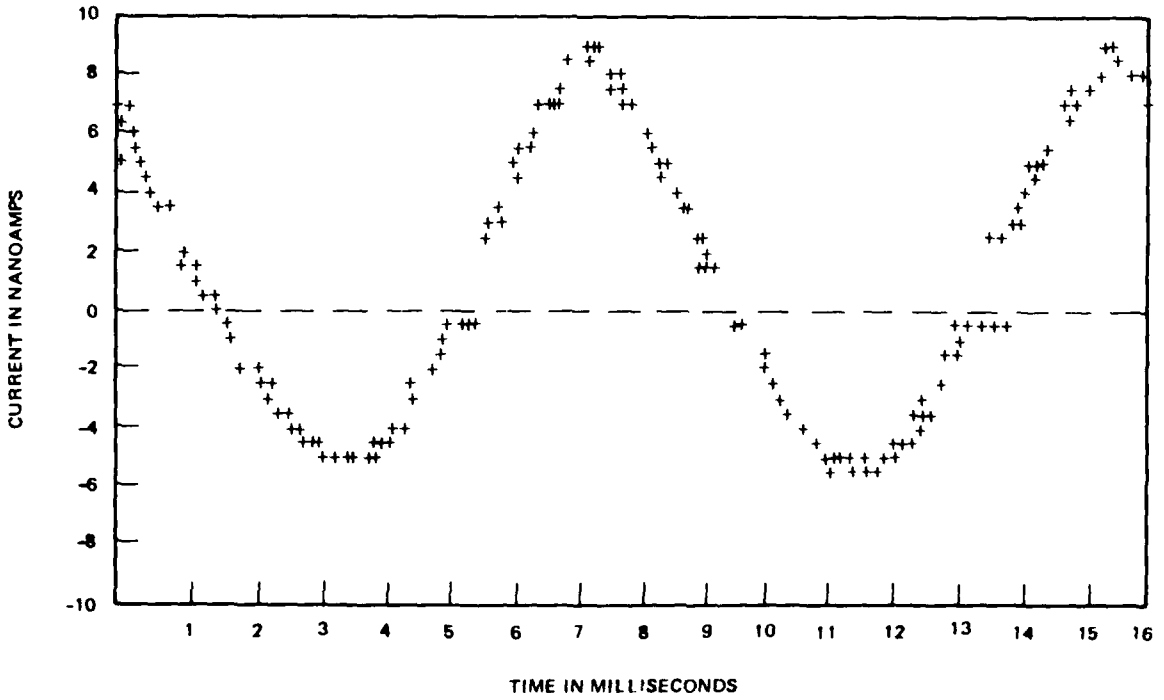


Figure 4. Current noise in S-3260 test system, 1 μA range on system 1

TABLE 7. TYPICAL PIN CONDITION SETTLING TIME DATA, 5400 DEVICES AT 25°C

Delay	1mS	2mS		3mS		5mS		10mS		100mS		1s*		10s*		Units
Parameter	Mean Value	Mean Value	% Chng from 1ms	Mean Value	% Chng from 1ms	Mean Value	% Chng from 1ms	Mean Value	% Chng from 1ms	Mean Value	% Chng from 1ms	Mean Value	% Chng from 1ms	Mean Value	% Chng from 1ms	
V_{CL}	253.5	254.8	1.0	250.5	0.8	250.7	0.7	250.8	0.7	250.3	0.6	247.4	0.4	246.7	1.0	mV
V_{CH}	2.793	2.792	0.1	2.793	0.0	2.793	0.0	2.793	0.0	2.794	0.0	2.853	0.1	2.857	0.2	V
I_{OS}	36.37	36.39	0.1	36.36	0.0	36.36	0.0	36.34	0.1	36.24	0.3	36.46	0.3	36.34	0.5	mA
I_{IH1}	4.53	4.54	0.2	4.55	0.5	4.56	0.7	4.57	0.9	4.56	0.7	4.80	0.6	4.89	2.0	μA
I_{IH2}	6.062	6.067	0.1	6.073	0.2	6.075	0.2	6.079	0.3	6.084	0.3	6.47	0.4	6.477	0.5	μA
I_{IL}	1.069	1.069	0.1	1.069	0.1	1.069	0.1	1.069	0.1	1.069	0.1	1.076	0.1	1.076	0.1	mA
I_{CCH}	4.746	4.742	0.1	4.743	0.1	4.740	0.1	4.740	0.1	4.74	0.1	4.74	0.1	4.804	0.1	mA
I_{CCL}	15.24	15.25	0.1	15.24	0.0	15.24	0.0	15.23	0.1	15.23	0.1	15.34	0.0	15.34	0.0	mA
V_{IC}	1.102	1.102	0.0	1.102	0.0	1.102	0.0	1.102	0.0	1.101	0.1	1.079	0.0	1.078	0.1	V

*These tests were run on only two devices. The percent change is calculated from the baseline measurements of the same two devices.

tendencies were observed in I_{OS} measurements and some V_{IC} and V_{OL} measurements, these parameters did not change as much as 3 percent, the value used as a significance guideline (Figures 5, 6, and 7). I_{IH} readings for Schottky parts rose significantly for longer delay times (Figure 8). This rise is attributed to device heating during prolonged testing. The I_{IH} results are nearly constant for pin condition settling times of 1 to 10 milliseconds. Limiting measurement to this range of pin condition settling time would ensure repeatable results. However, bench test methods require longer settling times and these longer times are more representative of devices in a hardware environment. This difference could be recognized by tightening the limits for I_{IH} and I_{CEX} when measured on ATE. Since measured I_{IH} values are well within specification over the entire temperature range, this approach would not greatly increase the number of rejected devices.

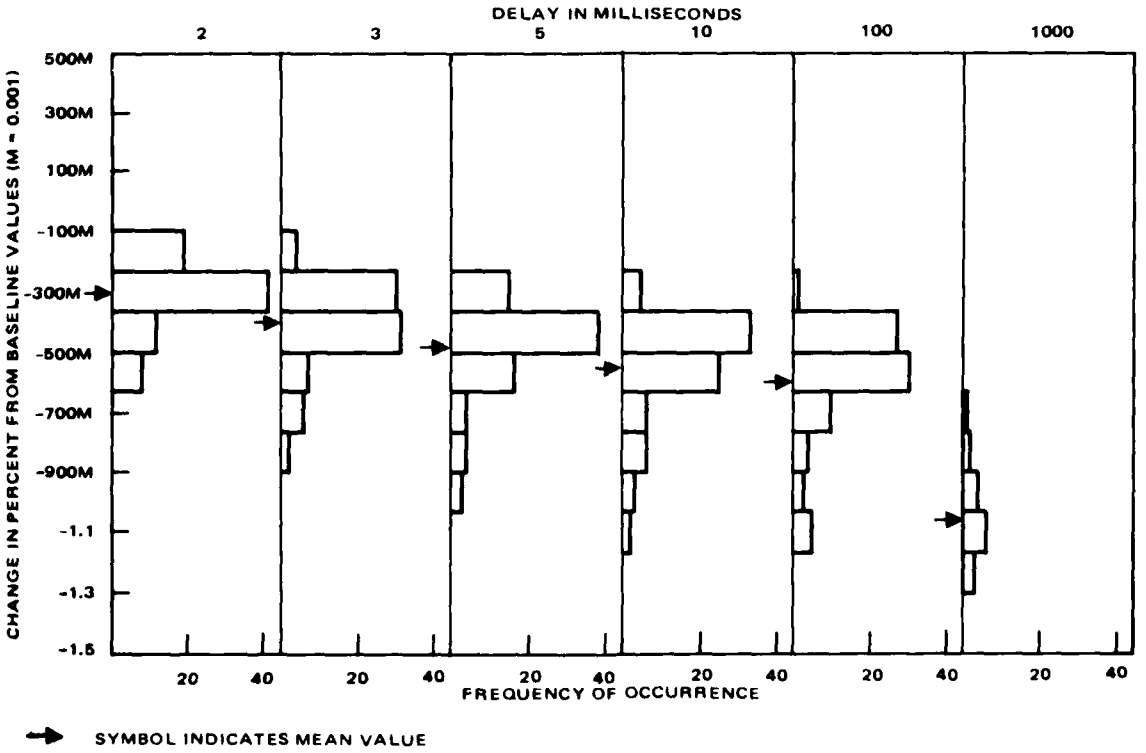


Figure 5. Histogram of pin condition settling time percent-change data for V_{OL} of 54S74 devices at 25°C

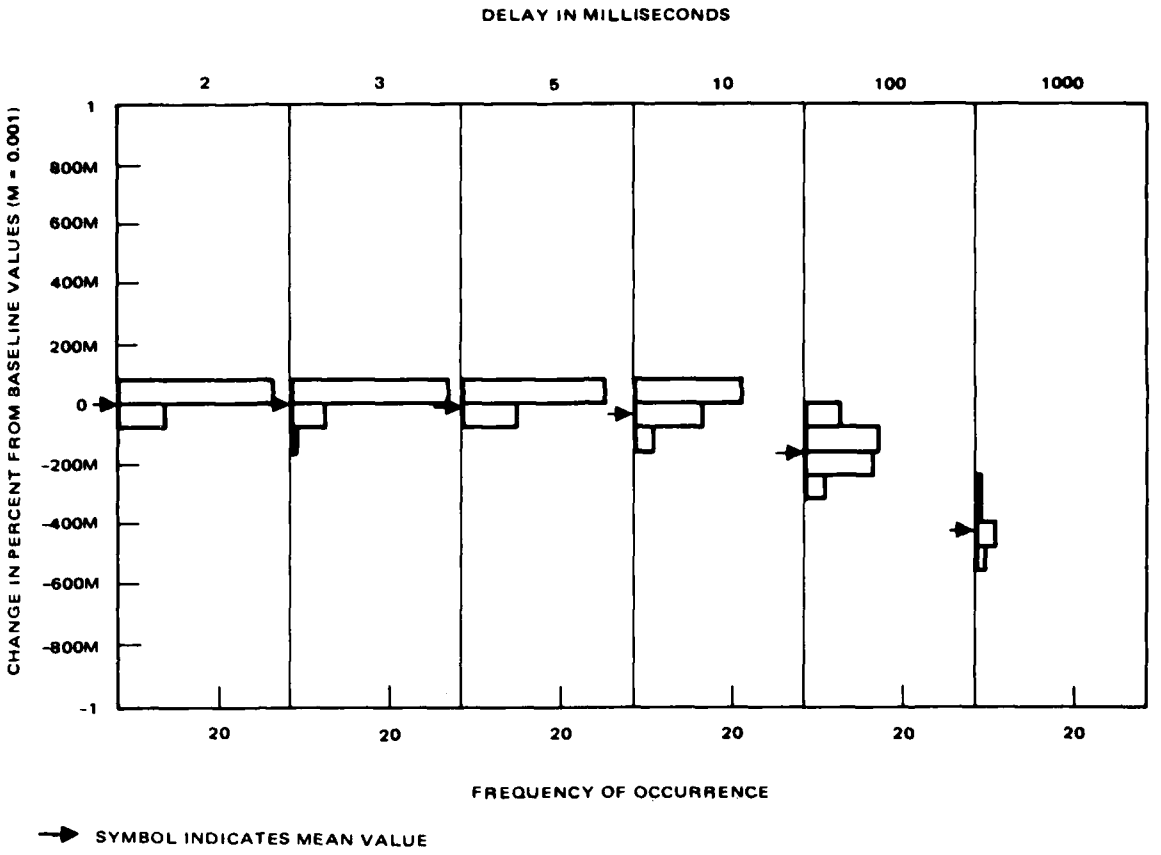


Figure 6. Histogram of pin condition settling time percent change data for I_{OS} of 54S00 devices at 25°C

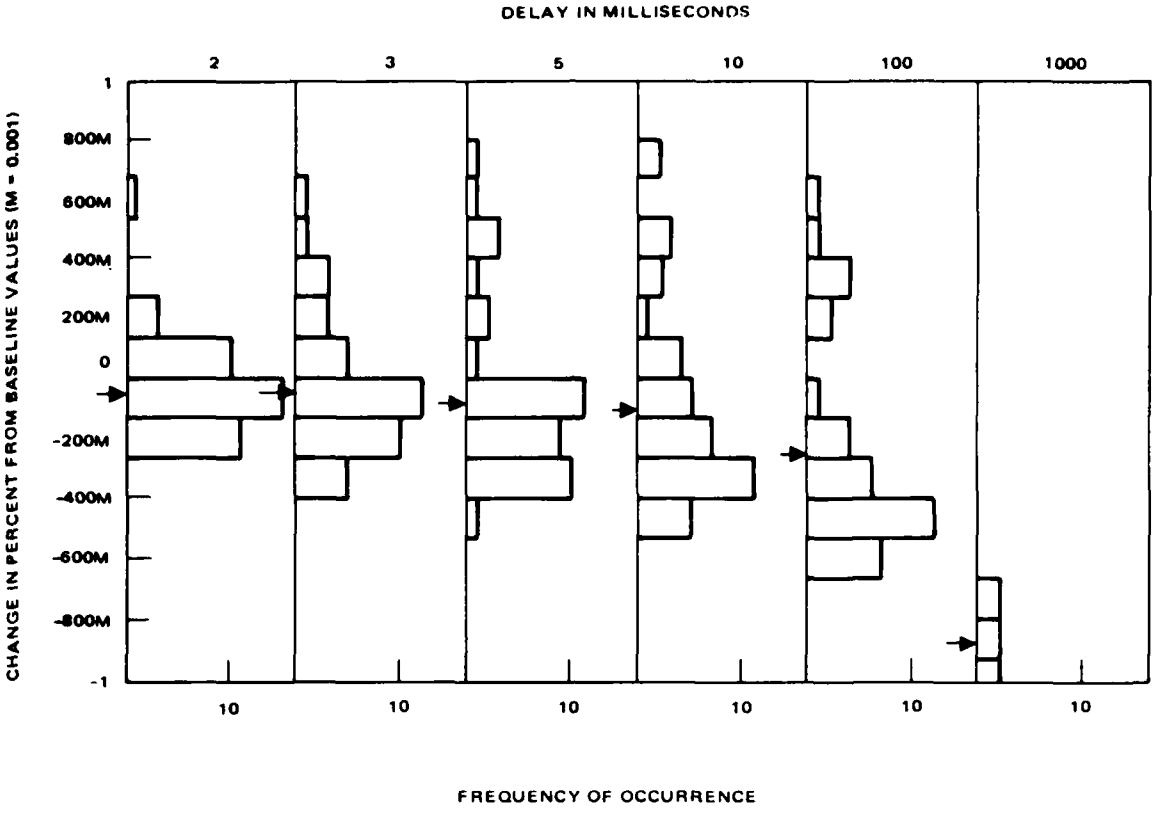


Figure 7. Histogram of pin condition settling time percent change data for V_{IC} of 54164 devices at 25°C

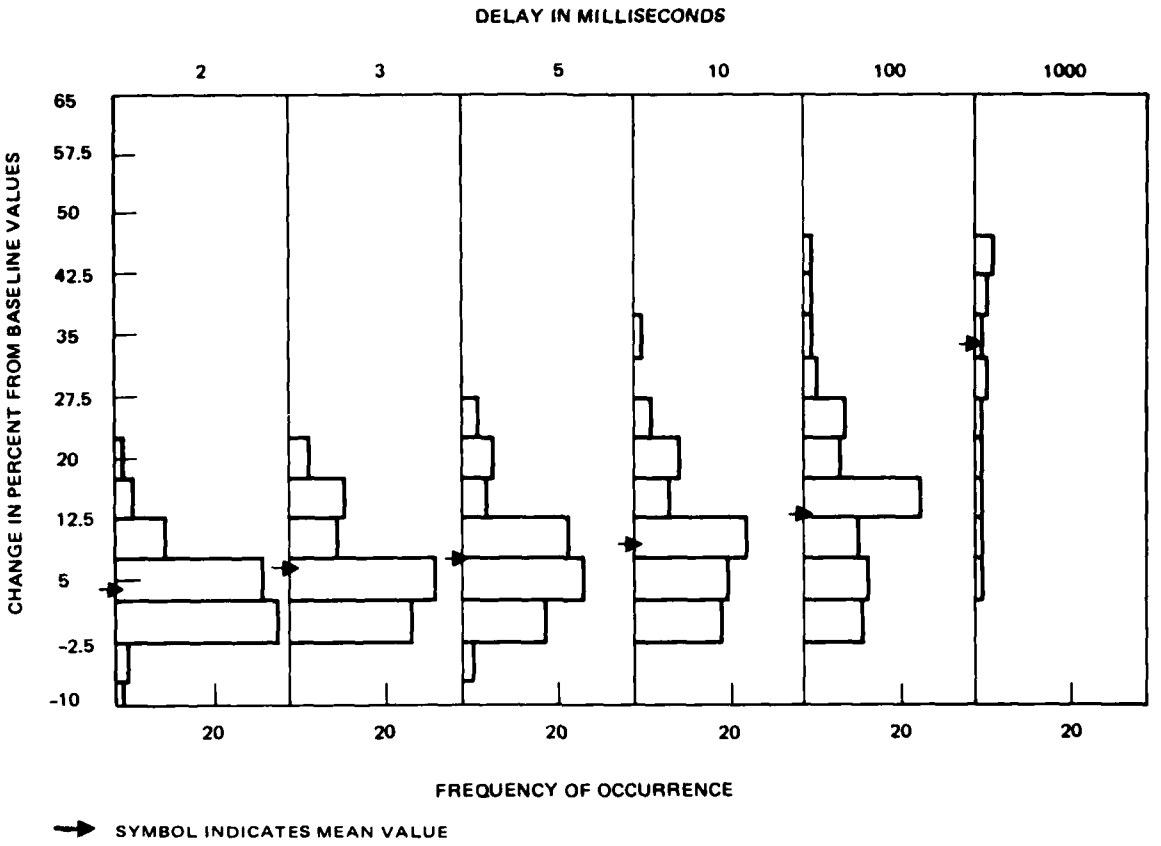


Figure 8. Histogram of pin condition settling time data for I_{IH5} of 54S74 devices at 25°C

5. EFFECTS OF MEASUREMENT SEQUENCE OF DIFFERENT DC PARAMETERS

TEST PROCEDURE

This study was designed to determine whether the sequence in which various parameters are measured affects the measured value. For example, does the I_{IH_1} value obtained when I_{III_1} is the first measurement performed differ from the value obtained when I_{III_1} is measured immediately after I_{OS}? The initial test programs were modified for this study. Parameters were measured on a single representative pin, each parameter measurement was made into a subroutine, and the algorithm discussed in Section 2 was used to generate the sequences in which the parameters were called. Figure 9 diagrams the program flow for this study.

RESULTS AND CONCLUSIONS

It might be expected that measurements sensitive to temperatures, when taken after measurements requiring high power dissipation (i.e., I_{OS}), would show a sequence sensitivity. This was not found to be the case. Table 8 shows that I_{CEX} and I_{IH} readings for each device under test (DUT) did not show a dependence on position with respect to I_{OS}. Indeed, no significant deviations were found during this portion of the study. Two factors which contribute to this sequence independence are the following:

1. Short measurement times and low duty cycles do not permit very much device heating, even during I_{OS} measurements.
2. ThermoStream® cooling (described in Section 6) minimizes device heating effects.

As was found in the pin condition settling time study (Section 4) and the differently defined ambient temperature study (Section 7), longer measurement times and a warmer thermal environment lead to device heating and a change in temperature sensitive parameters such as I_{IH} and I_{CEX}. To demonstrate this, I_{III_1} of the 54S00 devices was measured after I_{OS} tests in which the part was allowed 1 second for pin condition settling time during each I_{OS} measurement. The mean I_{IH} values measured were 40 percent greater than when measured after I_{OS} measurements with 1 millisecond settling times.

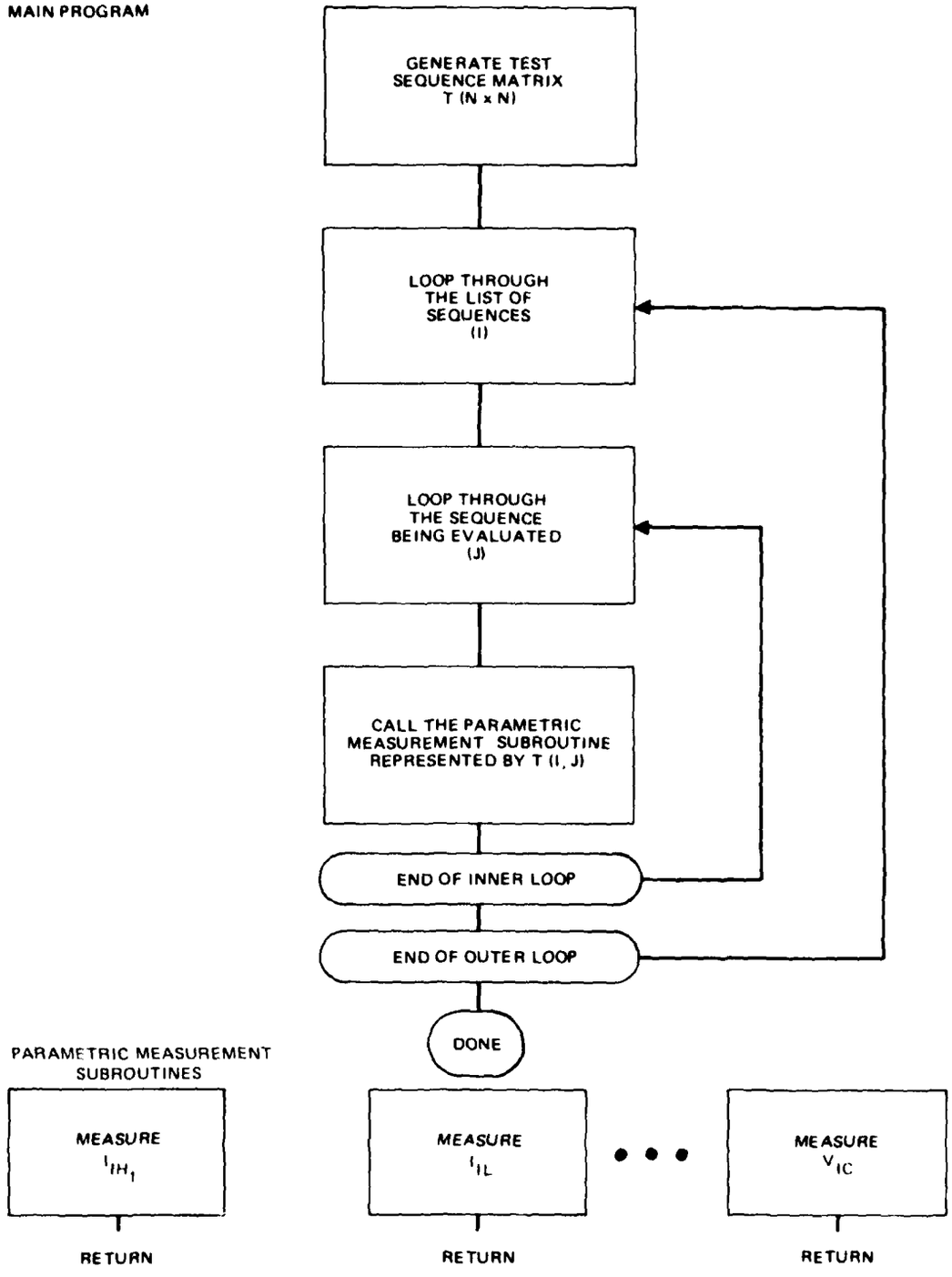


Figure 9. Flow of parameter sequence programs.

TABLE 8. SEQUENCE VARIATION OF TEMPERATURE – SENSITIVE PARAMETERS

	Measured Parameter			
	I_{IH_1}		I_{CEX}	
Device Type	Mean Value when Measured First	Mean Value when Measured After I_{OS}	Mean Value when Measured First	Mean Value when Measured After I_{OS}
5400	4.54 μA	4.55 μA	N/A[1]	N/A
54H00	5.83 μA	5.82 μA	N/A	N/A
54S00	51.2 nA	49.7 nA[2]	6.95 μA	7.02 μA
54LS00	16.2 nA	16.7 nA	N/A	N/A
5474	2.35 μA	2.36 μA	N/A	N/A
54H74	3.18 μA	3.17 μA	N/A	N/A
54S74	51.9 nA	53.7 nA	5.87 μA	5.84 μA
54LS74	15.5 nA	15.9 nA	N/A	N/A
54164	10.3 μA	10.5 μA	N/A	N/A
54LS245	17.8 nA	18.2 nA	N/A	N/A

1 N/A – Not Applicable

2 When a 1-second delay is inserted in each I_{OS} test, this figure increases to 69.7 nA – a 40 percent increase.

6. EFFECTS OF TEMPERATURE SEQUENCE

TEST PROCEDURE

Using the Temptronic TP450A ThermoStream® unit (Figure 10) to vary the temperature environment, all part types were tested as described in Section 3 at the three temperatures specified in the appropriate MIL-M-38510 slash sheet for the six combinations of three-temperature sequences. A programmed 30-second delay, accurate to within a few microseconds, was added to stabilize the DUT. The worst case temperature differential, +125°C to -55°C, was accomplished in less than 2 minutes under computer control. The high volume of air flow delivered by the ThermoStream® across the device under test maintains the temperature throughout the testing cycle. All temperature sequencing was also under computer control to ensure that all devices were tested under the same conditions.

RESULTS AND CONCLUSIONS

With this test technique, CMOS input currents exhibited unusual behavior, but their behavior was not sequence related. Rather, it was almost random. The problem was isolated to a bad reed in the MC-1 low current measurement option, and the tests were repeated using a spare unit.

CMOS, Schottky, and low-power Schottky leakage current (I_{IN}, I_{CEX}) readings taken at 125°C during retest exhibited a dependence upon previous temperature (Figure 11). Readings at 125°C were approximately 2° warmer when preceded by 25°C measurement than when preceded by a -55°C measurement. Increasing the stabilization time to 60 seconds reduced this dependence significantly. A similar difference was noted in 25°C readings. Those readings taken after 125°C readings showed larger leakage currents than those taken after -55°C readings (Figure 12). Again, increasing stabilization to 60 seconds reduced the difference. The discrepancies were caused by the devices not reaching a stabilized temperature when allowed only a 30 second wait. Also, no differences were noted in the -55°C data because the length of time required to cool to -55°C with the Temptronic TP450A provided a built-in delay adequate to stabilize the device under test. The differences caused by inadequate time at temperature were the only differences detected.

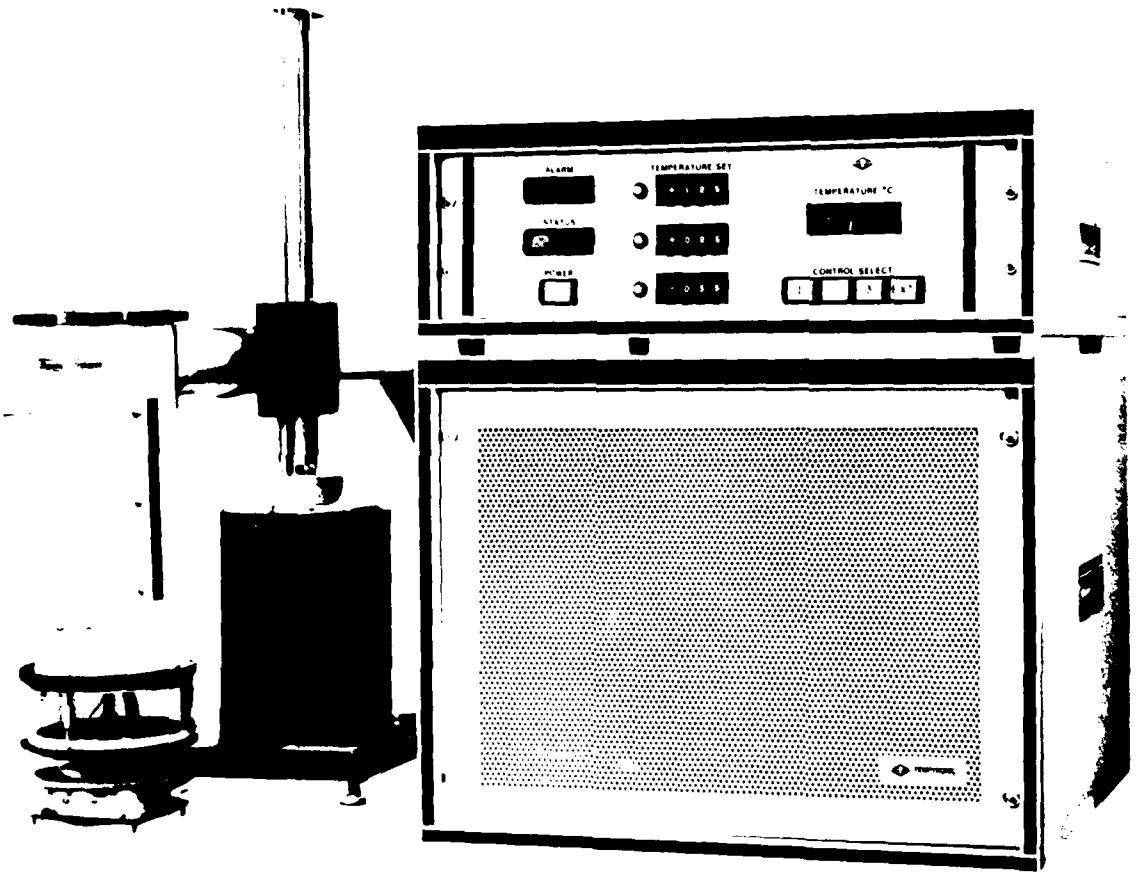


Figure 10. Temptronic TP450A ThermoStream® unit.

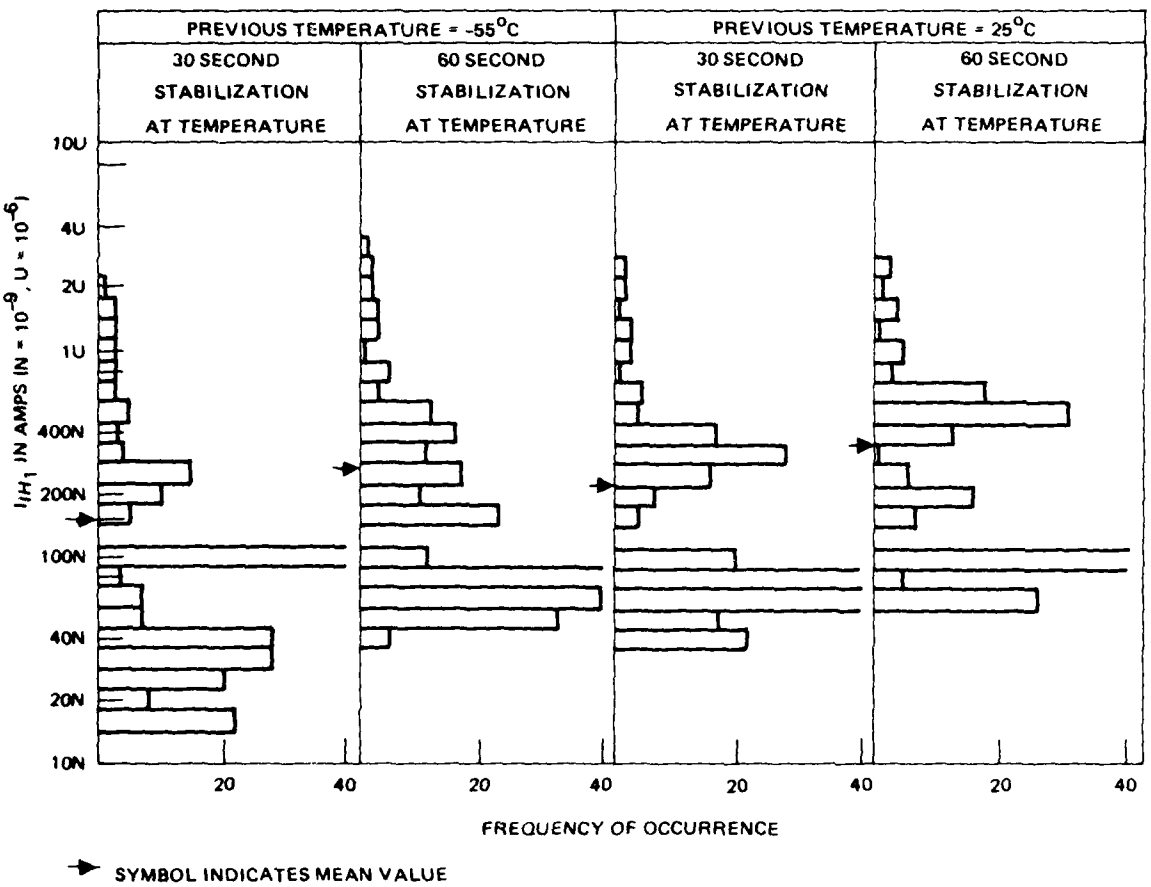


Figure 11. I_{IH_1} of 54LS00 devices at 125°C.

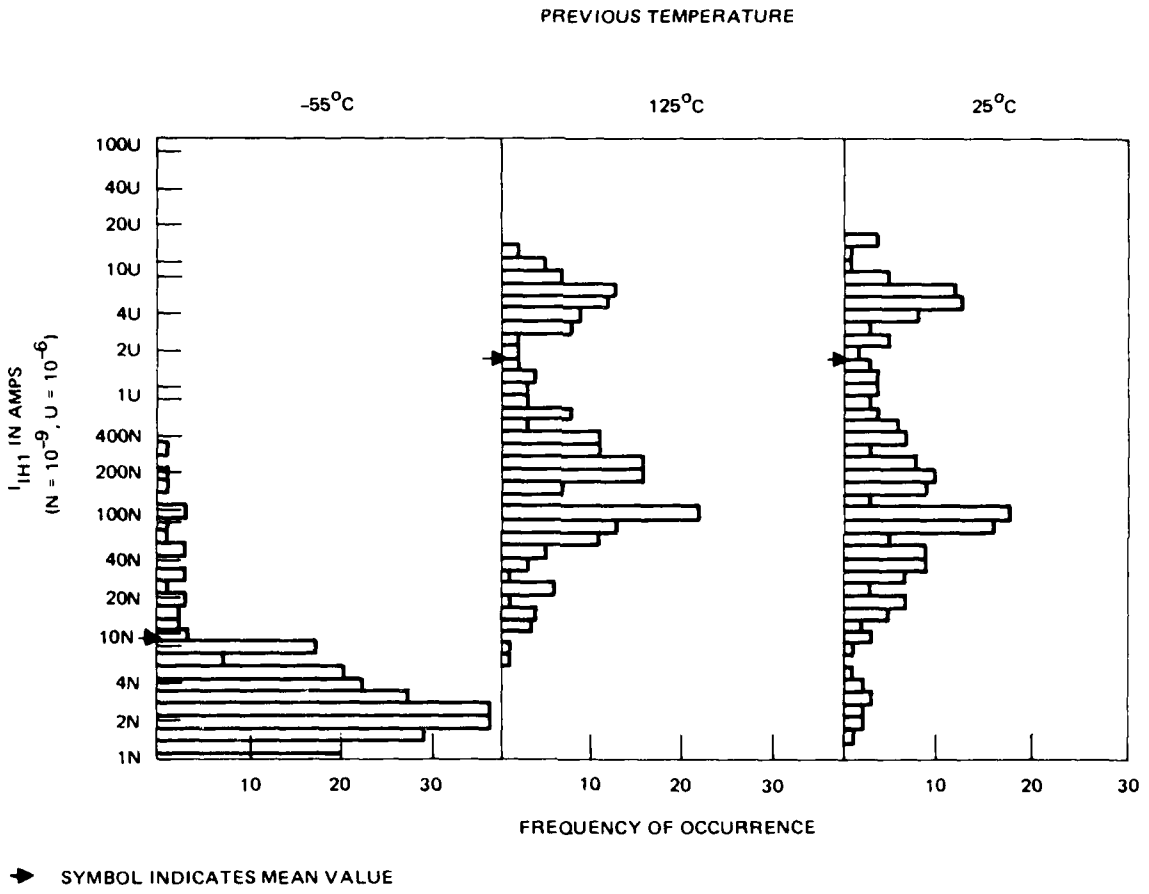


Figure 12. I_{III} of 54LS00 devices at 25°C after 30 second stabilization time from previous temperature.

ADDITIONAL TESTING

A short study to determine temperature differentials versus stabilization time by computing temperature from measured leakage current yielded the data shown in Figure 13. This method was used instead of the more accurate V_{FF} measurement to be described in Section 7 because large quantities of data had already been acquired which contained leakage currents but not V_{FF} data. The temperature was calculated from leakage currents rather than measured with a thermocouple because junction temperature, not case temperature, was desired. Since this data is very dependent on the thermal equipment used, its cooling and heating rates, and the flow rate of the airstream, the

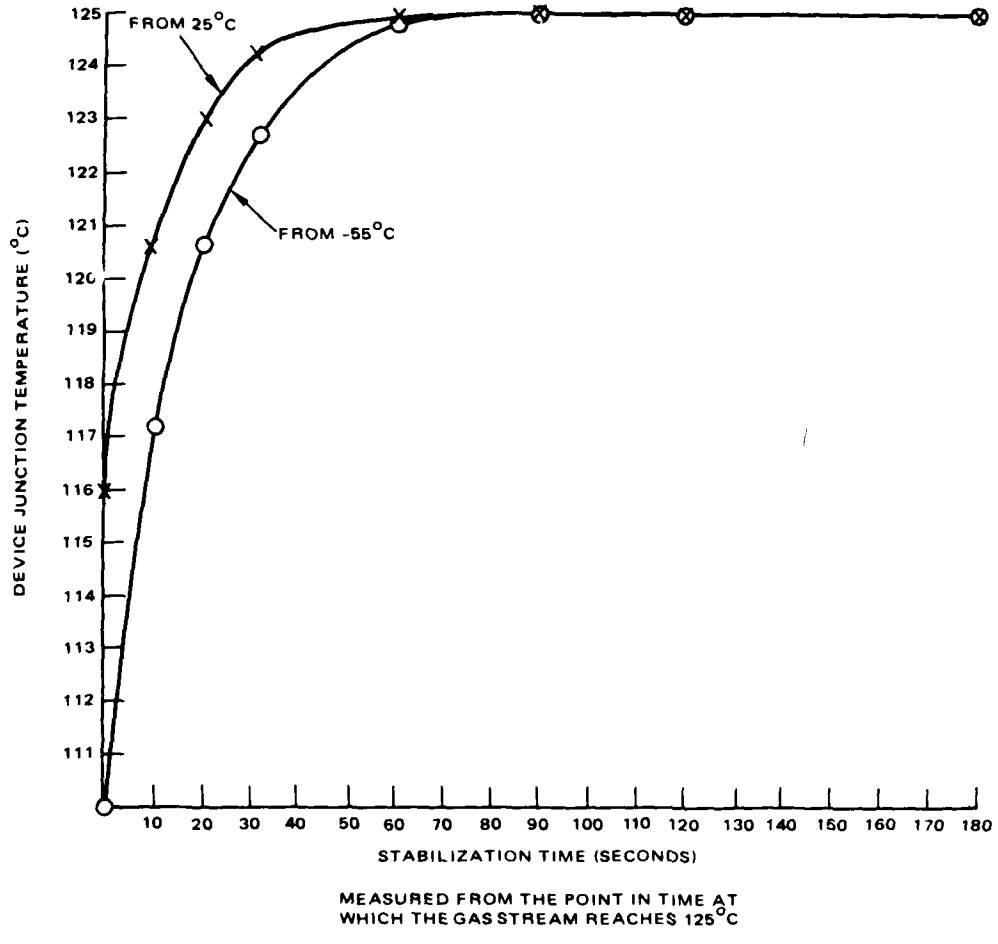


Figure 13. Temperature of the DUT versus stabilization time.

data is given for illustration only, and is not universally applicable. The flow rate of the TP450A was approximately 3 ft^3/min across the device.

7. EFFECTS OF DIFFERENTLY DEFINED AMBIENTS

TEST PROCEDURE

The effects of the differently defined ambient temperature environments were studied. All samples were tested, using the initial test programs and the four temperature environments defined below:

Method 1 — Still air temperature. The temperature of the DUT was stabilized using moving air, and then shutting off the airflow and making the measurements.

Maximum drift of the DUT temperature because of internal heating of the device is to be expected with this method. Relative humidity is kept below 40 percent by using dry nitrogen as the ambient atmosphere.

Method 2 — Moving air temperature (at least 50 ft/sec). This method uses a Temptronic TP450A ThermoStream® system with a dry nitrogen source to maintain relative humidity well below 40 percent. This method holds the temperature of the DUT closer to the ambient temperature called out in the test specification than Method 1. Some minor temperature drift occurs, depending on power dissipation, thermal resistance, and thermal time constant of the device.

Method 3 — Case temperature in still air. This method uses a thermal probe with thermal transfer cream applied to the probe tip for maximum thermal conductivity. Relative humidity is maintained below 40 percent by surrounding the DUT with a chamber that is purged by a small flow of dry nitrogen (see Figure 14). This method was used on two parts per vendor per slash sheet. Test results followed closely those from Method 1 when adequate soak time was given before shutting off the air flow.

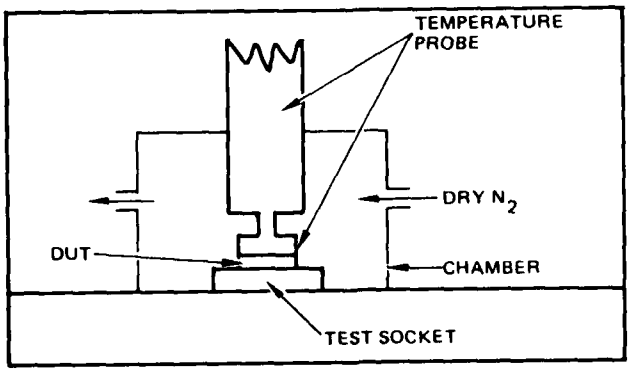


Figure 14. Chamber surrounding DUT to maintain relative humidity below 40 percent

Method 4 Case temperature in fluorocarbon. Especially for large volume testing, this is an alternative method for controlling T_C in still air. Because of the liquid-to-DUT interface, this method maintains DUT case temperature (T_C) closer to specified T_A than the other three methods. Relative humidity in the fluorocarbon bath is negligible.

V_{FF} MEASUREMENT

A modified V_{IC} measurement (designated V_{FF}) was used to indicate the relative drift of DUT chip temperature away from specified T_A as a function of differently defined ambient temperatures.

V_{FF} at an input pin (V_F of the input emitter-base diode, in parallel with V_F of the input clamp diode) varies with the internal temperature of the two diodes. Therefore, performing a V_{FF} measurement on one input pin of the DUT immediately before and immediately after the electrical test sequence gives an indication of how much the DUT internal temperature has drifted from the specified ambient temperature. To minimize internal heating from the VFF measurement, a forcing current of 2 mA is used.

RESULTS AND CONCLUSIONS

Before examining the test results, calculations were performed to estimate the temperature rises expected from the study. These estimates assume a θ_{JA} of 20°C/W for a 14 pin ceramic dual-in-line packaged device in fluorocarbon and θ_{JA} of 70°C/W in still air. These values are tabulated in Table 9 along with the temperature values obtained using the V_{FF} measurements.

The experimental data are consistently smaller than the estimates made. This is because the DUT did not reach equilibrium temperature during test. If the DUT were continuously retested, the data from the V_{FF} measurements would more closely correspond to the estimates. This was verified for the 54S74s, which after 10 minutes of continuous test time closed to within 0.5°C of the estimated values. For these devices, when equilibrium temperatures were reached in still air, the temperature differentials are large enough to influence propagation delay time measurements as well (Table 10).

For the CMOS parts in this study, the temperature rise in any of the test environments is very small, and no greater than the differential arising

TABLE 9. TEMPERATURE RISE IN DIFFERENTLY DEFINED AMBIENTS

	Calculated Temperature Rises (°C)		Measured Temperature Rises (°C)			
Device Type	Still Air	Fluorocarbon	Method 1	Method 2	Method 3	Method 4
5400	4.23	1.21	0.4	0.2	0.4	0.2
54H00	5.92	1.69	0.8	0.2	0.9	0.2
54LS00	0.82	0.23	0.2	0.1	0.1	0.1
54S00	6.65	1.90	1.1	0.3	1.1	0.2
4011A	<0.1	<0.1	0.1	0.0	0.1	0.0
5474	5.95	1.70	1.0	0.4	0.9	0.3
54H74	10.8	3.10	1.8	0.7	1.7	0.4
54LS74	1.44	0.41	0.3	0.1	0.2	0.1
54S74	11.6	3.30	2.1	0.6	2.1	0.5
4013A	<0.1	<0.1	0.2	0.1	0.1	0.0
54164	11.7	3.35	2.0	0.7	1.9	0.5
54LS295	6.83	1.95	1.1	0.4	1.1	0.3
4015	<0.1	<0.1	0.1	0.0	0.1	0.0

from bringing the part to temperature on two different occasions and taking measurements. For the Schottky parts, however, the temperature differential between still air and the moving gas or fluorocarbon bath is sufficiently large to cause changes in leakage current measurements.

For the 54H00 and the 54H74, the temperature differential between devices tested in a still-air environment and those tested in a fluorocarbon bath should increase both thermal leakage currents and I_{IH}. However, thermal diode leakage is only a small part of I_{IH} on these gold doped devices and no measurements on these devices are sufficiently temperature sensitive for the temperature rise to cause a significant parameter-measurement change.

While the remaining parts exhibit some small temperature differential between still-air and fluorocarbon testing, these temperature differentials are too small to affect parameter measurements.

The data indicate that both fluorocarbon bath and gas-stream testing produce similar results and that still-air testing results in higher junction temperatures with the differential being dependent upon device power dissipation. For the simple devices (small scale or medium scale integration) of this study, small parameter measurement variations occur for Schottky parts. However, no LSI parts were studied. This data should not be extrapolated to parts with higher power dissipations, such as a Schottky PROM, or to parts where test times are sufficiently long to enable T_j to reach thermal equilibrium, as in a 16K RAM. Rather, additional data must be obtained. It has been our experience that the junction temperature differential between still-air and the fluorocarbon bath is sufficient in bipolar RAMS at $-55^{o}C$ to cause parts to pass in still air and fail in the fluorocarbon bath.

TABLE 10. SCHOTTKY FLIP-FLOP PARAMETERS AS FUNCTION OF ENVIRONMENT AFTER STABILIZATION (10 MINUTE OPERATION)
Temperature Ambient (T_A = 125°C)

Parameter	Method 1 Still Air	Method 2 Thermo - Stream	Method 4 Fluoro-carbon	Fluorocarbon without 10 Min Device Operation	Units
T_{PLH_1}	8.36	7.96	8.32	8.16	ns
T_{PLH_2}	11.1	11.2	11.1	11.0	ns
T_{PHL_2}	9.48	8.86	9.00	8.97	ns
T_{PHL_3}	13.6	12.2	12.7	12.7	ns
T_{PHL_4}	8.12	7.50	7.71	7.64	ns
V_{OL}	297	300	299	300	mV
V_{OH}	3.021	2.955	2.940	2.939	V
I_{OS}	-69.25	-69.65	-69.55	-69.72	mA
I_{IH_1}	15.9	9.86	8.62	8.01	μA
I_{IH_2}	33.7	21.1	18.3	17.1	μA
I_{IH_3}	12.2	8.14	6.88	6.39	μA
I_{IH_4}	51.9	31.3	27.3	25.9	μA
I_{IH_5}	75.9	46.2	40.3	38.1	μA
I_{IL_1}	-1.46	-1.48	-1.49	-1.49	mA
I_{IL_2}	-3.84	-3.92	-4.01	-4.06	mA
I_{IL_3}	-2.86	-2.88	-2.90	-2.91	mA
I_{IL_4}	-2.80	-2.82	-2.83	-2.84	mA
I_{CC}	31.6	31.9	32.0	32.1	mA
I_{CEX}	2.34	1.53	1.32	1.21	μA

8. EFFECTS OF VARIABLE MEASUREMENT CONDITIONS

TEST DESCRIPTION AND PROCEDURE

This task began with an inspection of the MIL-M-38510 slash sheets and a listing of all conditions that could have ambiguous interpretations. Three potential problems were identified for investigation:

1. Pulse characteristics, such as rise and fall times and set-up and hold times are often defined only by a maximum or minimum time (i.e., $t_r \leq 10$ ns or $t_{set\text{-}up} \geq 20$ ns).
2. Input variables for functional tests are defined over a range of values (i.e., $V_{IL} \leq 0.8V$).
3. Clock rate or pulse repetition frequency for the functional or truth table test (subgroups 7 and 8) is not specified.

Because of past experience with many of these conditions, it was apparent that testing at 25°C would not be sufficient to provide the needed information. Therefore, these tests were performed at all three temperatures.

Examining Figure 15 shows that propagation delay times can be affected by input rise and fall times, and by the value used to trigger comparators to start and stop the timing measurements. The difference in the timing measurement t_{dif} is the difference between the time at which the input waveform crosses the actual input threshold of each device and the time at which it

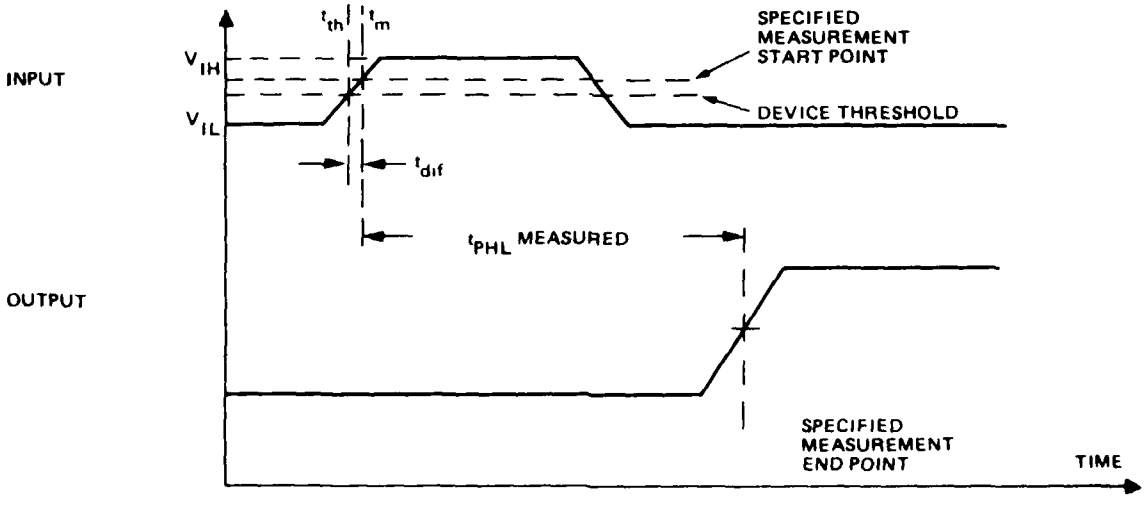


Figure 15. A t_{dif} error is included in measurements of time

crosses the assumed threshold upon which the measurement is based. This time difference is proportional to the voltage difference between actual and assumed threshold values and to the input rise or fall time. Since the rise and fall times are somewhat dependent on V_{IH} and V_{IL}, these values also become important.

Input rise and fall times were increased from 4 to 10 nanoseconds by capacitively loading the input drivers, and the devices were retested to the initial program. These results were then compared to the initial data.

Input variables for the truth table tests are loosely defined. Typically, input conditions such as $V_{IH_{min}} \leq V_{IH} \leq V_{CC}$ and $0 \leq V_{IL} \leq V_{IL_{max}}$ are permitted. Further, the pulse repetition rate is not specified. This allows results of truth table testing at pulse repetition rates approximating zero, using input signals with 0V to 5V swings, to be compared to results of testing with a pulse repetition rate (PRR) of f_{MAX} and input signal swings of $V_{IL_{max}}$ to $V_{IH_{min}}$. To demonstrate the resulting differences, the devices were tested by varying V_{IH}, V_{IL}, and PRR at the three temperatures.

RESULTS AND CONCLUSIONS

Increasing the input rise and fall times from 4 to 10 nanoseconds did not affect the timing data significantly. Figure 16 shows initial data and the data generated using increased rise and fall times for 54S74 devices. A Schottky device was chosen for illustration since any change in t_{dif} becomes a significant percentage of a time measurement.

While 5400 and 54H00 devices proved insensitive to V_{IL}, V_{IH}, and PRR variations, the 54S74 and 54LS295 devices demonstrated considerable sensitivity to V_{IL} and PRR at 125°C. A chart of V_{IL} versus frequency versus pass-fail at 125°C (Figure 17) illustrates that worst case testing ($V_{IL_{max}}$, $V_{IH_{min}}$, f_{MAX}) will fail many devices which pass less severe nominal testing. To ensure repeatability, V_{IL}, V_{IH}, and PRR must all be specified in narrower ranges. PRR could conveniently be specified either as 1 megahertz (which is an easily programmed value that is fast enough not to slow down test equipment and is standard for propagation delay measurements) or as the specified f_{MAX} limit if worst case is truly desired. In the latter case, it must be pointed out that many automated testers are not capable of performing the truth table test at f_{MAX}. Similarly, V_{IL} and V_{IH} must be specified over much tighter limits.

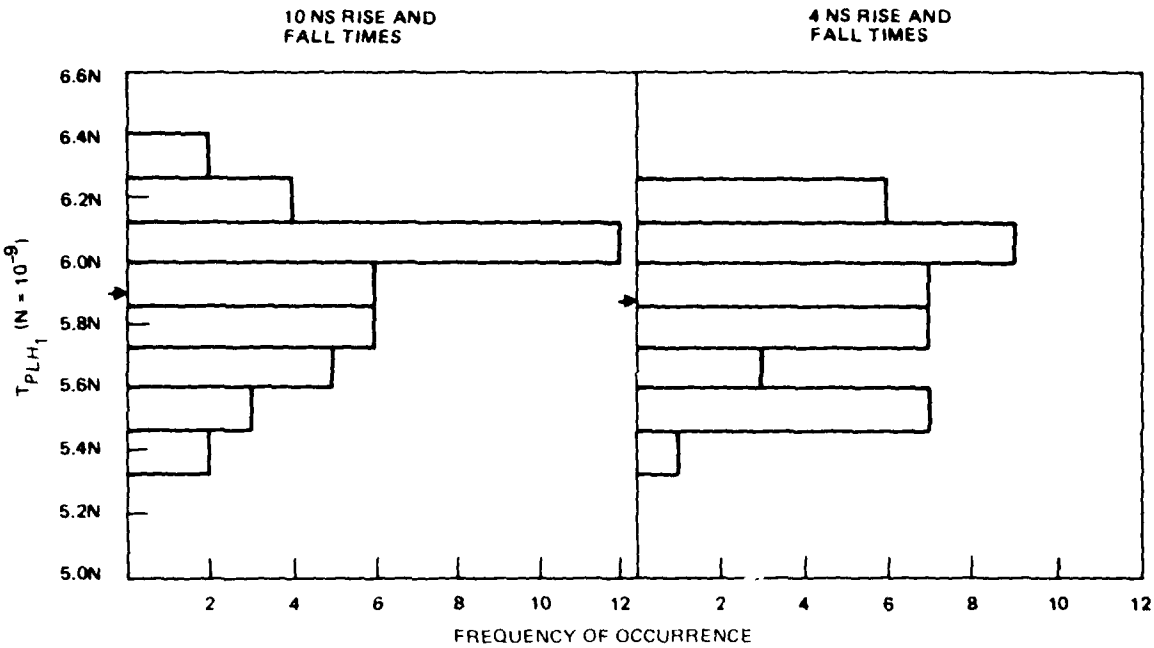
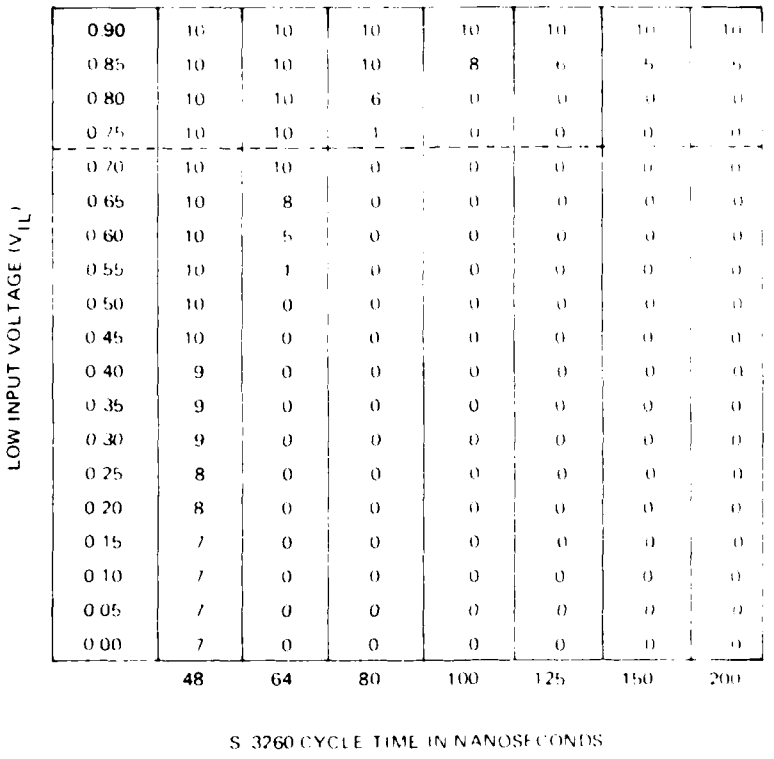


Figure 16. Histograms of T_{PLH_1} data for 54S74 devices at 25°C using standard (3.5 to 4 nanosecond) and 10 nanosecond rise and fall times.

Since the truth table tests are the only tests in Table III of the specification that can indicate whether the device meets $V_{IL_{max}}$ and $V_{IH_{min}}$ requirements dynamically, specifying that input levels be $V_{IL_{max}}$ and $V_{IH_{min}}$ would provide such an indication and assurance. By specifying the sequence of the propagation delay time measurements of Table III, subgroup 9 of the specifications, the truth table of the device can be tested without using the subgroup 7 tests. Therefore, if it is not intended that a $V_{IH_{min}}$ or $V_{IL_{max}}$ requirement be met, the truth table test of subgroup 7 could be deleted as redundant provided that the sequence in which the subgroup 9 measurements are made is specified and that this sequence covers all state changes of the DUT.



LOW INPUT VOLTAGE (V_{IL})	48	64	80	100	125	150	200
0.90	10	10	10	10	10	10	10
0.85	10	10	10	8	6	5	5
0.80	10	10	6	0	0	0	0
0.75	10	10	1	0	0	0	0
0.70	10	10	0	0	0	0	0
0.65	10	8	0	0	0	0	0
0.60	10	5	0	0	0	0	0
0.55	10	1	0	0	0	0	0
0.50	10	0	0	0	0	0	0
0.45	10	0	0	0	0	0	0
0.40	9	0	0	0	0	0	0
0.35	9	0	0	0	0	0	0
0.30	9	0	0	0	0	0	0
0.25	8	0	0	0	0	0	0
0.20	8	0	0	0	0	0	0
0.15	7	0	0	0	0	0	0
0.10	7	0	0	0	0	0	0
0.05	7	0	0	0	0	0	0
0.00	7	0	0	0	0	0	0

S 3260 CYCLE TIME IN NANOSECONDS

NOTES
1. Dashed line denotes V_{IL} specification limit
2. Ten devices were tested
3. V_{IH} 2.0V
4. Entries are number of devices failing the condition

Figure 17. Chart of V_{IL} versus truth table test frequency at 125°C for 54LS295 devices

9. EFFECTS OF SEQUENCE IN TIME MEASUREMENTS

TEST PROCEDURE

This study determined the effects of varying the order in which the timing measurements of Subgroup 9 in the specifications for flip-flops, counters, and a shift register are performed. The initial programs were modified by deleting the Subgroup 1 and Subgroup 7 tests and deactivating the temperature loops. The timing measurements were subroutined, and a comprehensive set of sequences of timing measurements were run.

RESULTS AND CONCLUSIONS

No effects of sequence in time were found in the data. Table 11 illustrates the similarity of the data from different sequences run on 54S74s and Table 12 similarly illustrates the 54LS295 data.

While no significant changes resulted from a change in test sequence, it is not clear that the MIL-M-38510 slash sheets adequately specify the preconditioning required before each test is run. Nor does MIL-STD-883, Method 3003.1, Paragraph 3.1 clarify this problem. Without additional preconditioning information, the test conditions are almost meaningless. For example, in MIL-M-38510/9C, Page 71 (Figure 18), after running Test 165, all outputs are in a low state. Before Test 166 can be run, Q_B must be brought back to a high state so that a high-to-low transition can occur. The specification shows a transition in Figure 8, but nowhere specifies what preconditioning is required to restore Q_B to a logic 1, or that preconditioning is necessary. If a high state is present at all outputs before Test 166, Tests 166 through 172 can be run in sequence without further preconditioning. Running in other sequences requires additional preconditioning. Therefore, it would be efficient to specify the order in which Subgroup 9 tests are to be run to minimize the additional preconditioning information required.

TABLE 11. REPRESENTATIVE 54S74 SEQUENCE IN TIME DATA

	Sequence Number						
Test Number	1	4	7	10	13	16	19
88	5.52	5.49	5.56	5.51	5.54	5.50	5.56
89	6.20	6.17	6.19	6.23	6.21	6.25	6.19
90	5.88	5.84	5.86	5.88	5.93	5.92	5.85
91	6.04	6.04	6.03	6.07	6.06	6.01	6.07
92	8.17	8.15	8.17	8.16	8.16	8.14	8.12
93	10.30	10.34	10.28	10.30	10.35	10.31	10.33
94	7.62	7.58	7.60	7.59	7.60	7.61	7.64
95	8.89	8.92	8.88	8.86	8.89	8.90	8.89
96	8.78	8.81	8.76	8.74	8.79	8.78	8.77
97	8.91	8.86	8.96	8.94	8.88	8.90	8.88
98	9.61	9.58	9.64	9.58	9.62	9.62	9.59
99	9.37	9.36	9.40	9.35	9.39	9.34	9.35
100	6.62	6.66	6.62	6.64	6.62	6.60	6.65
101	7.78	7.79	7.78	7.74	7.81	7.77	7.77
102	9.05	9.09	9.07	9.02	9.06	9.08	9.07
103	10.76	10.77	10.80	10.75	10.76	10.81	10.78
104	6.25	6.23	6.28	6.28	6.28	6.26	6.27
105	7.13	7.12	7.11	7.15	7.09	7.10	7.10
106	8.85	8.84	8.81	8.82	8.87	8.83	8.82
107	11.14	11.17	11.17	11.16	11.10	11.10	11.16

All data in nanoseconds. $T_A = 25^{\circ}C$

TABLE 12. REPRESENTATIVE 54LS295 SEQUENCE IN TIME DATA

Test Number	Sequence Number 1	5	9	13	17	21	25	29
81	23.6	23.3	23.4	23.6	23.6	23.4	23.5	23.5
83	25.0	24.4	24.7	24.4	24.9	25.0	24.6	24.7
85	23.4	23.5	23.2	23.6	23.4	23.4	23.4	23.5
87	23.5	23.2	23.3	23.7	23.3	23.2	23.5	23.4
89	22.0	23.2	22.9	22.7	22.2	22.3	22.4	22.8
91	22.0	23.1	22.8	22.6	22.2	22.3	22.4	22.7
93	21.4	22.7	22.3	22.2	21.8	21.8	21.9	22.2
95	21.2	22.7	22.1	22.2	21.9	21.8	21.8	22.0
97	25.7	26.1	25.2	26.6	26.1	26.6	25.3	26.0
99	25.8	26.3	25.4	26.7	26.2	26.7	25.3	26.1
101	13.9	13.7	13.8	13.8	13.8	13.6	13.8	13.6
103	13.8	13.8	13.7	13.9	13.8	13.8	13.7	13.7
105	24.7	26.3	24.5	23.1	26.3	26.6	25.4	23.2
107	23.6	25.2	23.5	22.2	25.3	25.5	24.3	22.2
109	20.5	21.1	20.6	20.3	20.3	20.1	20.1	20.9
111	20.4	20.3	20.3	20.2	20.2	20.2	20.0	20.4

All data in nanoseconds. $T_A = 25^{\circ}C$

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated are open, high level or low level)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D	Test No.	1 Input serial A	2 Input serial B	3 Q_A	4 Q_B	5 Q_C	6 Q_D	7 GND	8 Clock	9 Clear	10 Q_E	11 Q_F	12 Q_G	13 Q_H	14 V_{CC}	Meas terminal	Test limits Min	Test limits Max	Test limits Unit
7	Truth	3014		129	B	B	H	H	H	H	GND	A	A	H	H	H	H	4.5 V			See 4	
T_A = +25°C	table			130			H					B										
3, 6	test			131			L					A										
	5			132			↓					B										
				133				L				A										
				134				↓				B										
				135					L			A										
				136					↓			B										
				137						L		A										
				138						↓		B		↓								
				139								A		L								
				140								B		↓								
				141								A			L							
				142								B			↓							
				143								A				L						
				144								B				↓						
				145	↓	↓						A					L					
				146	A	A						A									See 4	
				147			↓					B										
				148			H					A										
				149				↓				B										
				150				H				A										
				151					↓			B										
				152					H			A										
				153						↓		B										
				154						H		A										
				155								B		↓								
				156								A		H								
				157								B			↓							
				158								A			H							
				159								B				↓						
				160								A				H						
				161								B				H	↓					
				162	↓	↓	↓	↓	↓	↓	↓	A	↓	↓	↓	H	H	↓				
				163	L	L	L	L	L	L		A	B	L	L	L	L					
8	Repeat subgroup 7 at T_A = +125°C and T_A = -55°C.																					
9	f_{MAX}	(Fig. 8)		164	IN	IN	↓	↓	↓	↓	GND	IN	4.5 V	↓	↓	↓	OUT	5.0 V	Q_D	11	----	MHz
T_A = 25°C	t_{PHL1}	3003 (Fig. 8)		165			OUT	↓	↓	↓	↓	GND	IN	↓	↓	↓	↓	↓	Q_A	12	4	ns
				166			↓	OUT	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	Q_B			
				167			↓	↓	OUT	↓	↓	↓	↓	↓	↓	↓	↓	↓	Q_C			
				168			↓	↓	↓	OUT	↓	↓	↓	↓	↓	↓	↓	↓	Q_D			
				169			↓	↓	↓	↓	↓	↓	↓	OUT	↓	↓	↓	↓	Q_E			
				170			↓	↓	↓	↓	↓	↓	↓	↓	OUT	↓	↓	↓	Q_F			
				171			↓	↓	↓	↓	↓	↓	↓	↓	↓	OUT	↓	↓	Q_G			
				172			↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	OUT	↓	Q_H			

Figure 18. MIL-M-38510/9C, page 71.

10. EFFECTS OF MEASUREMENT SEQUENCE OF THE SAME (DC) PARAMETER

TEST DESCRIPTION AND PROCEDURE

In Section 5, the effects of measurement sequence of different DC parameters are evaluated. In that study only a single pin was measured for each parameter. In this study the sequence in which the different parameters were measured remained as in the initial programs, but for each parameter the sequence in which appropriate pins were measured was varied. The resultant data was analyzed to identify any measurement dependence upon the sequence.

RESULTS AND CONCLUSIONS

No sequence sensitivities were encountered. Tables 13 through 15 give data for some parameters for the 54LS00, 54164, and 54H74 devices. As a note of caution, however, if V_{OH}, V_{OL}, or I_{OS} sequences are altered, preconditioning may be required just as in the propagation delay time sequences discussed in Section 9. Without this preconditioning, parts will fail V_{OH} and V_{OL} tests if they are in the wrong state. Although they may pass the I_{OS} test, the parameter measured will not be I_{OS} since the part will be in the wrong output state. Since some specification sequences do not require preconditioning and many other sequences do, it is important to specify that V_{OH}, I_{OS}, and V_{OL} tests be done in sequence in order to provide the required preconditioning.

TABLE 13. 54164 SEQUENCE OF SAME PARAMETER DATA FOR V_{OL}

	Sequence Number							
Pin	1	2	3	4	5	6	7	8
Q_A	211.8	215.4	212.4	211.4	211.5	213.7	213.3	212.1
Q_B	209.4	214.3	211.4	210.9	210.4	212.1	211.9	210.3
Q_C	211.7	218.3	210.0	211.7	211.7	213.4	213.1	212.4
Q_D	211.4	219.8	212.2	212.9	212.6	211.8	212.8	211.9
Q_E	211.4	216.3	211.8	210.7	212.3	213.2	211.7	213.1
Q_F	212.2	216.7	213.1	212.5	212.2	211.8	214.9	213.3
Q_G	212.7	216.6	212.8	211.9	212.0	212.9	214.2	214.6
Q_H	213.8	218.4	212.6	212.1	215.6	213.7	214.3	215.2

All data in mV. $T_A = 25^oC$

TABLE 14. 54LS00 SEQUENCE OF SAME PARAMETER DATA FOR I_{III}

	Sequence Number							
Pin	1	2	3	4	5	6	7	8
1A	2.23	2.33	2.25	2.28	2.18	2.28	2.38	2.23
1B	1.70	2.03	1.78	1.83	1.80	1.73	1.98	2.05
2A	2.18	2.10	2.20	2.25	2.15	2.20	2.28	2.23
2B	1.90	2.05	2.15	2.18	1.90	1.93	2.00	1.99
3A	2.00	2.23	2.18	2.23	1.93	2.03	2.08	2.05
3B	1.98	1.98	2.08	1.98	2.06	1.98	2.03	1.98
4A	2.15	1.98	2.10	2.03	1.98	1.95	2.05	2.03
4B	1.73	1.80	1.95	1.85	1.83	1.80	1.83	1.78

All data in nA. $T_A = 25^oC$

TABLE 15. 54H74 SEQUENCE OF SAME PARAMETER DATA FOR V_{IC}

	Sequence Number							
Pin	1	2	3	4	5	6	7	8
D1	-0.869	-0.870	-0.867	-0.868	-0.869	-0.870	-0.867	-0.868
Clock 1	-0.866	-0.866	-0.867	-0.865	-0.866	-0.864	-0.863	-0.867
Clear 1	-0.844	-0.842	-0.843	-0.844	-0.845	-0.844	-0.846	-0.843
Preset 1	-0.848	-0.845	-0.848	-0.847	-0.848	-0.846	-0.847	-0.848
D2	-0.861	-0.859	-0.861	-0.861	-0.860	-0.862	-0.859	-0.861
Clock 2	-0.861	-0.860	-0.862	-0.862	-0.859	-0.861	-0.860	-0.860
Clear 2	-0.840	-0.843	-0.842	-0.842	-0.840	-0.840	-0.842	-0.841
Preset 2	-0.845	-0.846	-0.843	-0.845	-0.844	-0.845	-0.845	-0.846

All data in volts. $T_A = 25^{\circ}C$

11. EFFECTS OF PIN APPLICATION SEQUENCE

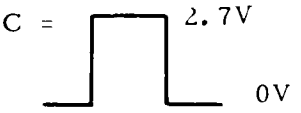
TEST DESCRIPTION AND PROCEDURE

All tests in Subgroups 1, 7, and 9 were run with a comprehensive set of pin condition application sequences within the constraints of the specification. Since it was considered mandatory to connect GND and V_{CC} at the beginning of each test run to avoid damaging CMOS devices, we followed this practice rather than including them in the pin application sequence. Taking V_{OH} test numbers 1 through 4 as an example from MIL-M-38510/30102, we have the following pin conditions for tests 1 through 4.

TABLE 16. V_{OH} TEST PIN CONDITIONS (D-TYPE FLIP-FLOP)

Pin	CLR	D	CLK	PR	Q	$\overline{Q}$
Test 1	0.7 V	2.0 V	GND	2.0 V		-0.4 mA
Test 2	2.0 V	2.0 V	GND	0.7 V	-0.4 mA	
Test 3	2.0 V	2.0 V	C 1/	2.0 V	-0.4 mA	
Test 4	2.0 V	0.7 V	C	2.0 V		-0.4 mA

1/



The conditions whose sequence of application were varied were 0.7 V, 2.0 V, GND or C, and -0.4 mA.

RESULTS AND CONCLUSIONS

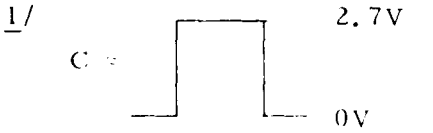
Whenever valid data was obtained, it showed no dependence on pin application sequence. However, a random pin application sequence, especially with clocked data, does not necessarily lead to valid data. In tests 3 and 4, if the clock pulse is applied before input conditions are established on D, the outputs may assume the complement state, resulting in improper test conditions for a V_{OH} measurement. In addition, in devices where outputs

are fed back to gates that drive the complement output (such as this flip-flop), the application of the load to the output after input conditions are stabilized, or after the connection of a voltmeter (a capacitive short), can frequently cause the output to change state, resulting in invalid data.

Since this procedure left open the question of damage or inconsistent data which was thought to occur by including V_{DD} and ground in the pin application sequences, an additional study was required. The CD4011A and CD4013A parts were tested by establishing a variety of 0V and 15V input conditions and then connecting ground or V_{DD} and later running the initial program to check for damage. The parts were again tested by establishing these input conditions with V_{DD} and ground, both first at 0V and then at 15V, before being switched to their appropriate values. No damage and no parameter changes were noted. However, no testing was performed to evaluate the effects of these voltage conditions on the lifetime of the devices. The absence of damage to the CMOS gates and flip-flops is attributed to the gate structure as well as to advances in input protection circuitry.

The following suggestions are made:

1. Pulsed inputs could be defined such that pulses occur after establishing dc conditions. This can be done in the MIL-M-38510 specifications in the notes that follow Table III. For example in Table 16, note 1 can be expanded to



applied after other conditions are established at CLR, D, and PR terminals.

2. Output states should be checked and re-established if necessary after forcing currents are applied and measurement systems are connected. This can be done in a suggested new paragraph in MIL-STD-883 to cover conditions unique to ATE as explained in Section 16, Suggestions for MIL-STD-883.

12. EFFECTS OF UNDESIGNATED PIN AMBIGUITY

TEST DESCRIPTION AND PROCEDURE

Undesignated pins are frequently allowed to be either open, logic high, or logic low, at the discretion of the test engineer. This is the case with /05703, /00205, /00903, /02203, /07001, /07101, /30001, and /30101. The remaining five device specifications require undesignated pins to be open. In each measurement where an undesignated pin was allowed to be high, low, or open, the measurement was made five times, with the undesignated pins set to V_{CC}, logic high (2.0V), logic low (0.7 or 0.8V), ground, and open. Although the device with open input pins typically performs as expected, connecting input pins to either a high or a low state input voltage greatly decreases the susceptibility to noise spikes. This is particularly true of low-power Schottky and CMOS devices where small quantities of charge can cause changes of state.

The state of undesignated output pins can also affect the data. In counters and shift registers, the states of unmeasured output terminals are often unspecified. Loading unmeasured outputs during I_{OS} tests affects the current available to the measured output as well as the junction temperature of the DUT. In the special case of shorting more than one output at a time, as is allowed in Table III of the specifications, the absolute maximum power dissipation rating of the device is exceeded.

RESULTS AND CONCLUSIONS

Varying the undesignated input pin conditions did not produce significant variations in measurements of DC parameters. When varying the conditions of the input pins such that undesignated outputs were switched, some propagation delay time measurements were affected.

Varying the conditions of undesignated output pins was found to affect the data in two situations. In the first situation, propagation delay times for 54164 and 54LS295 shift registers varied with the number of outputs making a state transition during the measurement cycle. The worst case T_{PHL_1} for the 54164 occurred when all of the outputs started in a high state and were cleared together. This case yielded a T_{PHL_1} with a mean value of 37.5 nanoseconds. When only one output was in a high state before being

cleared. T_{PHL_1} was found to be 35.1 nanoseconds, 6 percent smaller than the first case. For the 54LS295, a similar but smaller change was noted. The respective mean values were 26.4 ns and 25.4 ns. A 1 nanosecond change was the limit used as a significance guideline. These differences could be avoided by specifying all output state changes that are to occur during the measurement.

The second situation is the I_{OS} test. Table 17 illustrates how I_{OS} varies with the loading of the other outputs. For the 54LS295, the measurement with all outputs grounded is 39 percent smaller than the measurement with only the measured output grounded.

Since loading more than one output at a time results in a power dissipation beyond the absolute maximum rating of the device, this situation can be rectified by specifying that only one output be grounded at a time. A proposed change in MIL-STD-883B, Method 3011 to cover this situation is discussed under the topic, "Additional Conditions for I_{OS} Measurements," in Section 15.

TABLE 17. EFFECT ON I_{OS} OF GROUNDING MORE THAN ONE OUTPUT

Device Type	I_{OS} (mA) Number of Additional Grounded Outputs				Maximum Difference (%)
	0	1	2	3	
54LS295A	-42.8	-42.5	-32.7	-26.0	39
5400	-46.7	-46.2	-45.5	-44.9	4
54H00	65.5	64.9	62.6	-57.0	13
54S00	69.1	67.4	-66.3	-55.7	19
54LS00	26.1	-26.0	25.9	-25.8	1

$T_A = 25^{\circ}C$

13. INVESTIGATION OF MEASUREMENT EFFECTIVENESS

Investigations were undertaken to examine the effectiveness of tri-state timing measurements, to find alternatives to the currently specified f_{MAX} tests, and to look for a method of examining C_{in} on CMOS parts on a general purpose automated test system such as the S-3260.

TRI-STATE TIME MEASUREMENT INVESTIGATION

Enable and disable times of tri-state outputs have been a bane to engineers using automated test equipment. Minimum capacitance on the output of an S-3260 with a comparator connected is slightly under 30 pF. When a load is connected, the capacitance increases to between 45 and 50 pF. Many commercial specifications require probe and jig capacitance of as little as 5 pF. MIL-M-38510/30606, Rev B requires 15 pF minimum for t_{HZ} and t_{LZ} measurements. Thus, it is very difficult to make the specified t_{HZ} and t_{LZ} measurements. Also, in the military specification, these same two measurements require comparator trip points of V_{OH} minus 0.5V and V_{OL} plus 0.5V. On a bench with an oscilloscope, the dynamic V_{OH} and V_{OL} levels are easily seen, but on ATE there is some complication.

Following are three methods that have been used on ATE for measuring the specified t_{HZ} and t_{LZ}:

1. Measuring DC values. This gives a false impression of output voltages that occur while operating at rated speed, especially if care is not taken to approximate the actual load.
2. Measuring dynamic levels. Output comparator reference levels are adjusted until the device fails a functional test. With this method, the measurement still depends upon where in the waveform the output is compared. In Figure 19, three different VOH values are obtained from the same waveform. The value obtained depends upon the start time (t_B) and stop time (t_B') gating the comparator.
3. Assuming V_{OH} and V_{OL} as worst case full load values permitted by the specification (that is, 2.4V and 0.4V). This is a more stringent requirement than either other method, but it is so much easier to implement that it has found some acceptance.

While all three methods give some information about the output transistors of the DUT, the circuit conditions during test have little relation to those

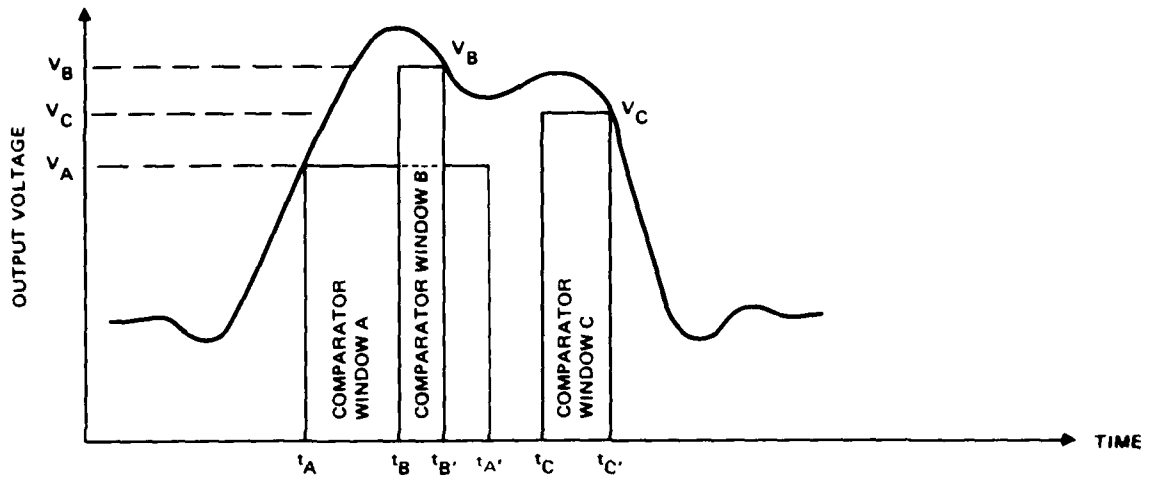
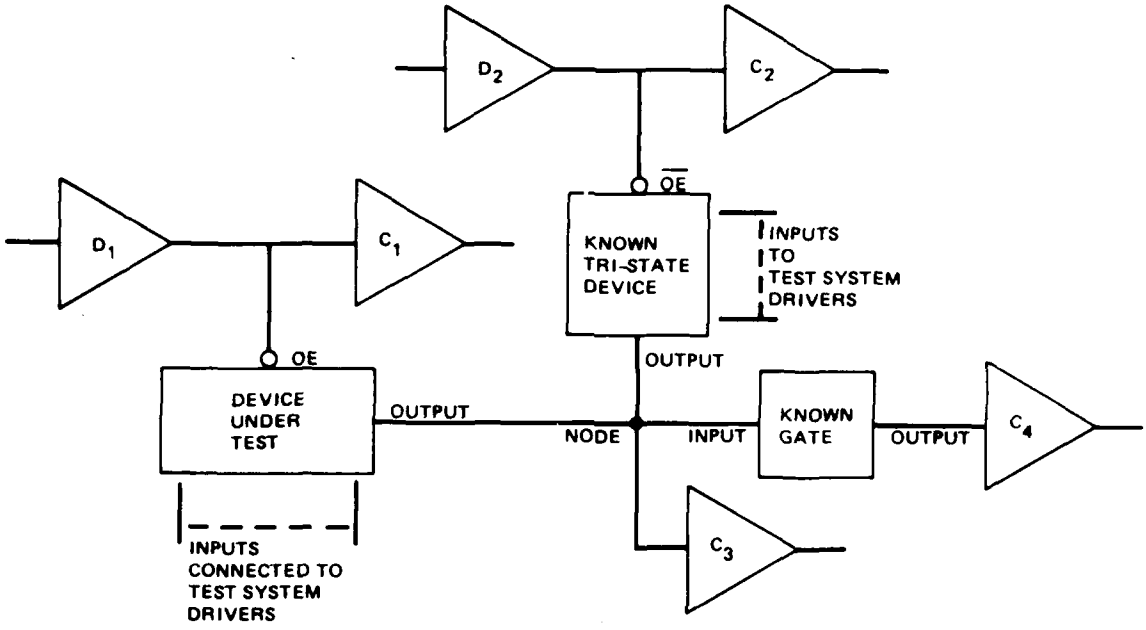


Figure 19. Result of dynamic volt measurement dependent on timing characteristics of comparator window.

encountered in actual use. The designer needs an idea of the capability of the device to release a bus (t_{HZ} and t_{LZ}) or to be enabled and drive another device (t_{ZH} and t_{ZL}).

One solution to the designer's problem, which removes some of the constraints imposed by ATE, is to connect the tri-state outputs to a bus structure. The node of this artificially created bus is connected to the DUT output, the output of a previously characterized tri-state device, and the input of a gate (Figure 20). The characterized tri-state device is capable of driving the gate input, as is the DUT. Bus access time (t_{ZH} and t_{ZL}) are then measured as the time between an output enable pulse at the DUT and a change of output state of the known gate minus the previously measured delay of the gate. The gate is preset by the known tri-state device. Since the timing of this device has also been characterized, it can be made to access or release the bus node at any desired time. Bus release times (t_{HZ} and t_{ZL}) are measured by attempting to access the bus with the known tri-state device after the test equipment attempts to disable the DUT at its output enable (OE) terminal. A bus conflict is created when two or more devices attempt to force different logic levels on the bus. An increase in the delay time from the known device enable signal to the gate output indicates that the DUT has not released the bus. The bus release time



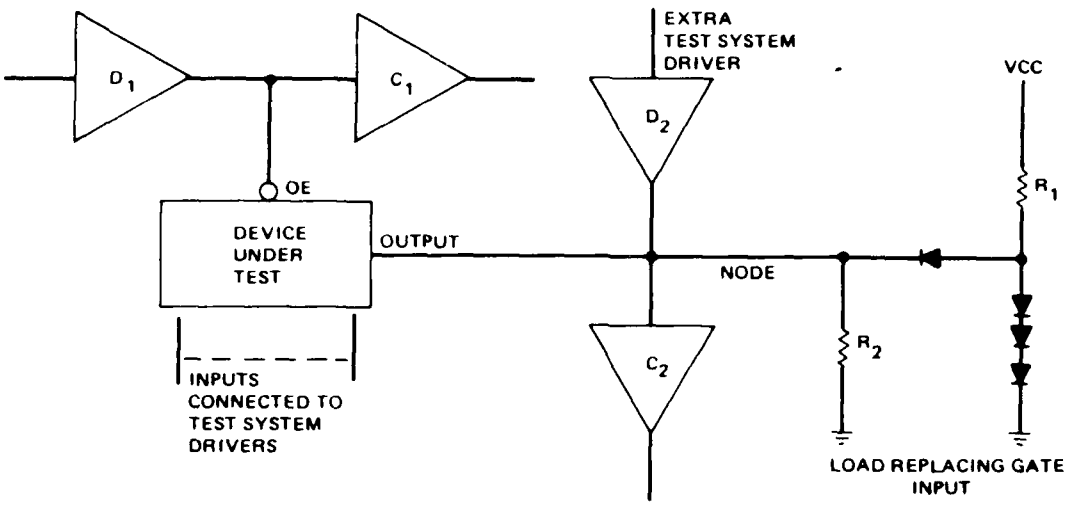
$D_1 = D_2$ = TEST SYSTEM DRIVERS OR PULSE GENERATOR

$C_1 = C_2 = C_3 = C_4$ = TEST SYSTEM COMPARATORS

Figure 20. Theoretical alternative to tri-state measurements.

would be the difference between the time at which the DUT OE terminal was switched to disable the DUT output and the earliest time that the known device could access the bus without a conflict. This test method presents some problems to the test engineer who implements it. Bus elements (the known tri-state device and gate) need to be available as a load at each tri-state output of the DUT. The measurement requires the subtraction of an external gate delay. It also requires that several additional signal sources and comparators be connected. Some of these connections are to points other than DUT terminals.

Some of the problems might be eliminated by letting a driver (pulse generator) of the ATE become the known device trying to access the bus, and replacing the known gate with a passive network as is done in propagation delay measurements. Such a situation is presented in Figure 21. Now



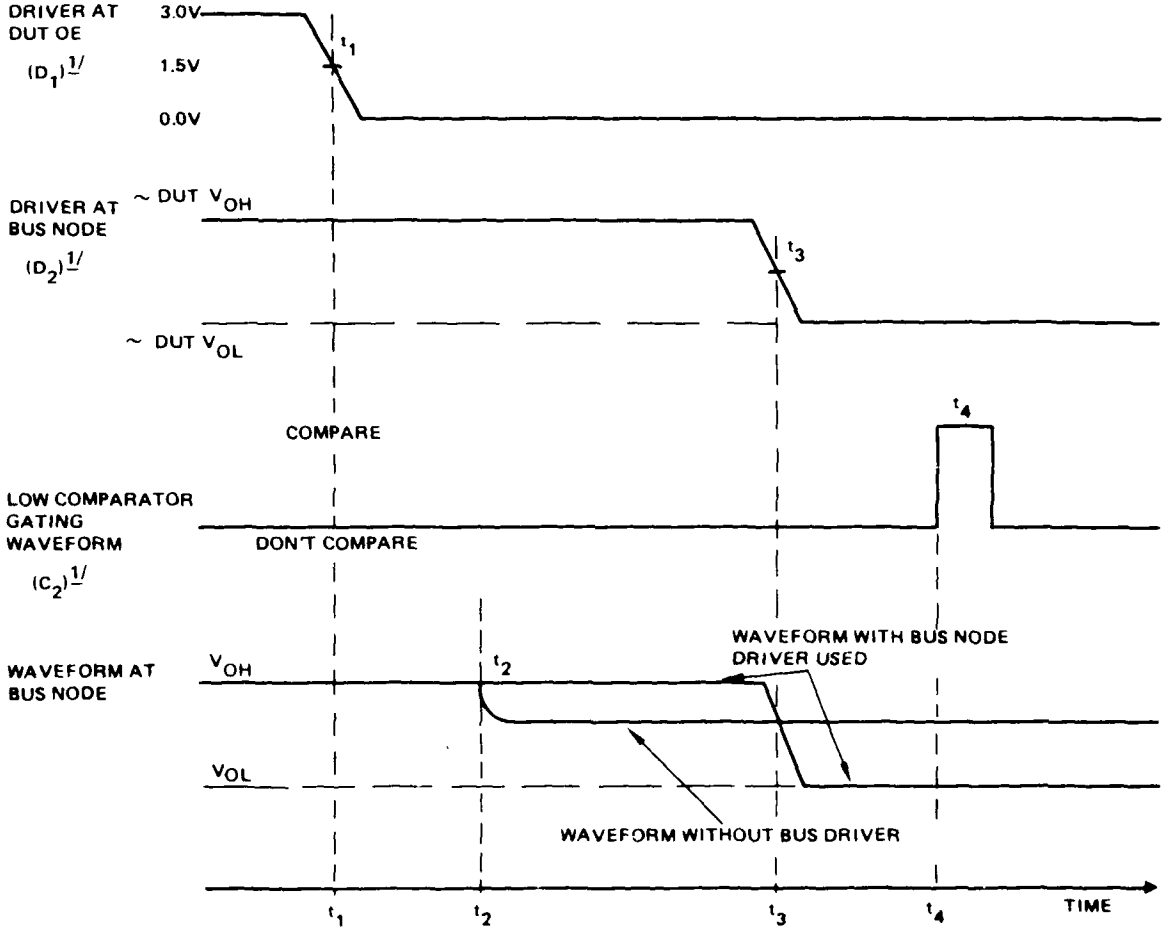
D_1 - D_2 TEST SYSTEM DRIVERS OR PULSE GENERATOR
C_1 - C_2 TEST SYSTEM COMPARATORS

Figure 21. ATE model of Figure 20.

system timing can be adjusted to determine bus access and release times for the DUT, and no precharacterized devices are required. Since only the newest ATE permits its drivers to act as tri-state devices, implementation of this scheme on most ATE, including the S-3260, requires great care to ensure that the system driver on the bus node and the DUT output create minimum conflict on the bus. The approach taken was to activate the driver when it could clearly be done without conflict (after a disable, before an enable), and then walk the driver pulse start or end time toward a point of conflict with the DUT output. When a comparator indicates that both the driver and the DUT output are attempting to force the bus node in opposite directions, the measurement value has been determined. Examples of this method are given for t_{HZ} and t_{ZH}. The test method for t_{LZ} would follow that for t_{HZ} except for the levels of some waveforms. The method for t_{ZL} would similarly follow that for t_{ZH}.

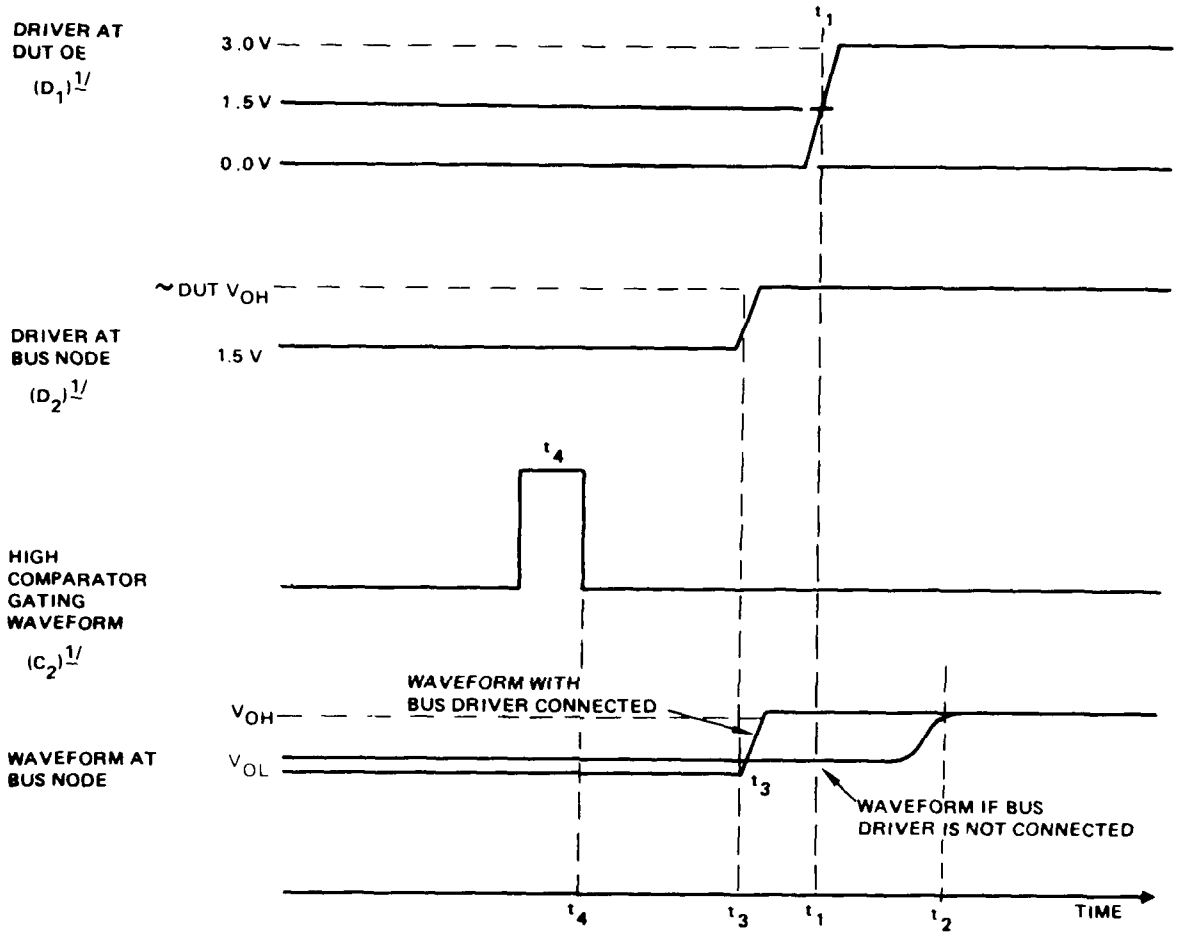
Figure 22 illustrates the initial timing of the test setup for a t_{HZ} measurement. The driver at the bus node has its logic 1 set at approximately the DUT V_{OH} level and its logic 0 set at approximately the DUT V_{OL} level. It is desirable to approach actual DUT levels, but exact matching is not required since small differences in the programmed value will affect driver loading but will not damage either the driver or the DUT. The switching of the driver (t_3) is set to occur well beyond the suspected output disable time. The comparator logic 0 reference (locompare) level is set as close to the bus driver low level as possible without inadvertently triggering the comparator. A programmed value of 50 mV greater than the driver low level was found to be satisfactory. The comparator window time (t_4) is initially well beyond t_3 so that the comparator is not initially triggered by the falling edge of the bus driver signal. The test program reduces the value of t_4 (moving t_4 closer to t_3) until a fail indication is received, signaling that the comparator is detecting the falling edge of the bus driver waveform. At this point t_4 is incremented by 1 nanosecond so that the comparator will again indicate a pass condition. This timing relationship between the falling edge of bus driver waveform (t_3) and the comparator start time (t_4) is maintained throughout the test. Both t_3 and t_4 are reduced simultaneously 1 nanosecond at a time (moving closer to t_2) until a comparator fail indication is received. This fail indication results because the device output has not fully disabled and is still applying a forcing voltage to the bus. The measured t_{HZ} would then be $t_3 - t_1 + 1$ nanosecond. The 1 nanosecond is added because the DUT had not released the bus at t_3, but has successfully released the bus during the last pass at $t_3 + 1$ nanosecond.

Figure 23 illustrates the initial waveforms for a bus access time (t_{AH}) measurement with the bus driver set at a low level of 1.5V and a high level approximating the DUT V_{OH} level. The switching time t_3 is fixed and is used as a reference during this measurement. The high comparator trigger level is set 50 mV above 1.5V. Initially t_4 is earlier in the test cycle (smaller) than t_3. However, t_4 is incremented until a pass is recorded, and then decremented 1 nanosecond. The driver at the DUT OE terminal is initially set



NOTE: 1/ NOTATION AS IN FIGURE 21.

Figure 22. Initial waveforms for suggested t_{HZ} measurement.



NOTE: 1/ NOTATION AS IN FIGURE 21.

Figure 23. Initial waveforms for suggested t_{ZH} measurement.

to switch at a time t_1 sufficiently late to ensure that the DUT will not attempt to access the bus (t_2) until after t_3. At this time t_1 and thus t_2 are decremented until a pass signal is generated at the comparator, and the bus access time measurement (t_{ZH}) is measured as $t_3 - t_1$ nanosecond.

In practice, this method yielded results comparable to the measurements specified in the MIL-M-38510 specifications. The data in Table 18 shows

TABLE 18. COMPARISON OF SUGGESTED TRI-STATE METHOD TO SPECIFICATION METHOD

54LS295 Parameter	Temperature (°C)	Specification Method (ns)	Suggested Method (ns)
t_{ZL}	25	23.78	20.11
	-55	27.88	24.42
	125	25.70	22.08
t_{ZH}	25	13.51	10.47
	-55	13.93	10.81
	125	15.25	12.03
t_{LZ} [1/]	25	24.75	22.37
	-55	25.22	22.91
	125	29.20	27.15
t_{HZ} [1/]	25	18.49	16.03
	-55	19.16	16.57
	125	19.66	16.98

[1/] Specification requires a minimum load capacitance of 15 pF. A 50 pF load capacitance was used for the specification method data.

that enable and disable time readings were 2 to 3 nanoseconds faster using this method (the DUT does not need to charge or discharge an external 50 pF load, but only a load sufficient to affect the edge of the system driver waveform).

The ability of a system driver to simulate the limited drive capability of a tri-state output has properly been questioned. An S-3260 driver can source -100 mA in the high state (-170 mA when shorted to ground) and can sink +100 mA in the low state. This I_{OL} value is almost double that of a Schottky bus driver such as a 54S240, and the I_{OH} value is much greater than the -12 mA sourced by the 54S240. When compared to the values of a 54LS295, the I_{OL} and I_{OH} values of a system driver are an order of

magnitude greater. This greater current capability affects the measurements in two ways. First, the higher drive capability makes system capacitance less important since the capacitance is more rapidly charged and discharged. Second, the higher drive capability makes it more difficult for the DUT to affect the waveforms and trigger the comparators. Indeed, some difficulty was encountered in choosing appropriate comparator levels to obtain sensitivity to waveform changes without allowing the comparator to be falsely triggered by noise. The addition of a passive network to buffer the driver would enable the driver to more closely emulate the drive capability of the DUT output and thus reduce the difficulty in choosing comparator levels. On an S-3260, the addition could be accomplished by changing load modules. This approach should be examined further.

The suggested method differs from the current specification in that the intent is to describe the performance of the DUT in a bus environment rather than to measure the characteristics of the output drivers of the DUT. It does require programming effort to implement, but is less sensitive to system capacitance. Since system capacitance limitations make the current t_{HZ} and t_{LZ} measurements very difficult to implement, this is a definite advantage.

MAXIMUM FREQUENCY TEST INVESTIGATION

As discussed in Section 3, many slash sheets require functional tests with clock rates exceeding the maximum test frequency of the ATE (20 to 25 MHz, depending on the test system). Although test system capabilities are growing with each new generation of ATE, component speeds are increasing even faster. With the recent introduction of a 100 MHz tester came the introduction of advanced Schottky parts with an f_{MAX} of over 200 MHz. Thus, the test engineer is faced with a dilemma. If he does not test f_{MAX}, he may be passing parts that cannot meet end use requirements since the part which passes one-shot propagation delays or a 1 MHz truth table test may not pass with all timing parameters simultaneously exercised

to their limits. Since the test engineer can rarely afford to bench test 100 percent of the devices, his alternatives are the following:

1. Forget that a problem exists and drop the f_{MAX} test completely
2. Implement the test, keeping all timing relationships as tight as required by the specification except that clock rate is reduced to the test system capability
3. Implement the test as specified, at great expense, through special fixturing or bench methods
4. Bench test some fraction of a lot for f_{MAX}
5. Rather than measuring f_{MAX} directly, measure some additional timing parameters and calculate an equivalent f_{MAX}.

The second and fifth methods might be acceptable both to the manufacturer and the reliability engineer if some evidence existed to support the conclusion that results produced by these methods would correlate with those produced by the f_{MAX} test implemented to the specification. The second method only produces a pass-fail indication at the programmed clock rate. This cannot be correlated to the pass-fail indication of the specification f_{MAX} test without testing parts which marginally fail f_{MAX}. No such parts were among those procured for the study. In support of the second method, it is better than no f_{MAX} test at all and should detect many f_{MAX} failures. It is the method most often implemented in an ATE environment.

The fifth method produces a value for f_{MAX}, and this value can be compared to measurements of f_{MAX} taken on the bench. For a D-type flip-flop, such as the 54S74, data setup and hold times are measured and f_{MAX} is calculated as the inverse of either of the following:

logic 1 setup time + logic 1 hold time + t_{PDLH} from CLK to $\overline{O}$

or

logic 0 setup time + logic 0 hold time + t_{PDHL} from CLK to $\overline{O}$,

whichever produces a lower f_{MAX} value. This fifth method was implemented in the /07101 and /02203 programs used throughout the study. These devices were then bench tested for f_{MAX}. The S-3260 calculated values were within 4 percent of actual f_{MAX} at 25°C (Table 19). The methods did not produce similar results at temperature extremes, although neither method indicated any device failures among the tested devices. One explanation for the differences at temperature extremes is that the calculated f_{MAX} did not use a measured minimum data pulse width along with the

TABLE 19. COMPARISON OF S-3260 F_{MAX} TEST TO SPECIFICATION TEST

Device Type	Temperature ($0^{o}C$)	Specification Test (Method 3) (MHz)	S-3260 Test (Method 5) (MHz)
07101	25	91.5	95.3
	-55	83.4	97.9
	125	85.6	118.1
02203	25	45.4	46.9
	-55	36.2	47.0
	125	38.4	60.8

set-up and hold times. The simplified formula used was not adequate. However the data obtained by the alternate method, when it includes a measured data pulse width, is sufficiently useful that it has been incorporated in a number of programs when bench testing is deemed impractical.

MEASUREMENT OF INPUT CAPACITANCE

Alternatives to the direct measurement of input capacitance on CMOS devices were sought. Since test system capacitance was so much larger than the capacitances to be measured, no suitable alternative was discovered. As mentioned previously (Section 3, Table 4), C_{in} measurements were not part of the baseline programs used in the bulk of the study for this reason.

14. DEFINE "OPEN" AND "GROUND"

TEST DESCRIPTION AND PROCEDURE

This task was divided into two subtasks. Subtask 1 characterized various ground and signal paths of the S-3260, using a Hewlett Packard 4271B 1 MHz LCR meter to determine what "open" and "ground" conditions are seen by a DUT. Resistance, inductance, and capacitance of each path were measured using the LCR meter. Since some of the resistances to be measured exceeded the highest measurable value on this meter, a conductance meter with a resolution of 10 picosiemens was used for these resistances. Measurements of less than one unit on this meter are interpreted as resistances greater than 10^{11} ohms.

Subtask 2 required adding resistance, capacitance, and inductance to the system at DUT inputs and at the DUT ground terminal in order to seek a range of acceptable values that could be used to define "open" and "ground" conditions.

RESULTS AND CONCLUSIONS

The results of the first subtask appear in Table 20. Figure 24 is included to aid in locating some of the measurement points. The capacitance and parallel resistance values limit the quality of the open condition. The inductance and, to a smaller extent, series resistance values affect the ground condition. The smallest supply path inductance for a DUT after decoupling is 50 nH; that is, 12 nH from the decoupling capacitor to the DUT V_{CC} terminal, plus 38 nH from the other lead of the capacitor to the DUT ground terminal. This value assumes no inductance in the ceramic decoupling capacitor.

The second subtask was further divided. Additional resistance to ground and capacitance were added to DUT inputs in an attempt to find a worst case open condition, and additional inductance was placed in ground paths to study the ground condition. For the open condition, the additional capacitance (200 pF maximum) at DUT inputs served only to slow the rise and fall times of the system drivers and had no effect on conditions requiring some inputs to be open (such as V_{IC}). The initial test program, as

TABLE 20. INDUCTANCE OF GROUND PATHS AND CAPACITANCE OF THE S-3260

From	To	Measured Capacitance Value (pF)	R	Condition[1/]
DT	SG	29	$>10^5$ megohms	O
DT	SG	31	$>10^5$ megohms	I&O
DT	SG	44	$>10^5$ megohms	I&O, C5
DT	SG	31	$>10^5$ megohms	I&O, C30
DT	SG	35	$>10^5$ megohms	I&O, L1
DT	SG	36	$>10^5$ megohms	I&O, L2
DT	SG	40	$>10^5$ megohms	I&O, L1, L2
DT	SG	49	$>10^5$ megohms	I&O, L1, C5
DT	SG	36	$>10^5$ megohms	I&O, L1, C30
	Measured Inductance	(nH)	Milliohms	
DG	SG[2/]	81	13	Hardwired
DG	LG	126	20	L1
SG	LG	52	9	L1
DT	driver	146	24	I&O
DT	SG	335	54	O
DT	SG	222	35	I&O
DT	LG	263	43	L1
DT	LG	285	49	L2
DT	SG	206	33	L1, L2
DT	SG	161	26	L1, L2, I&O
DG	ground ring at point nearest V_{CC}	38	6	Hardwired
DT	bottom of socket	12	3	

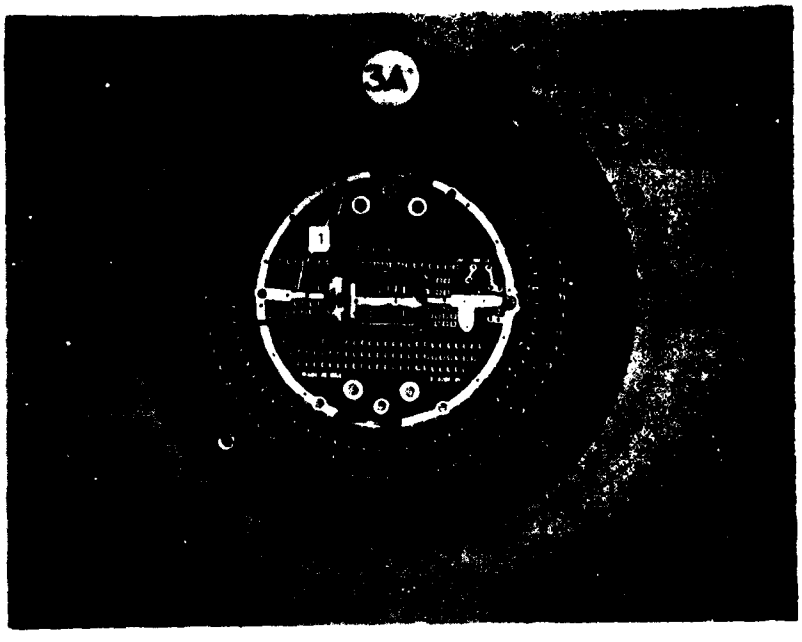
[1/] The following abbreviations are used:

SG - Ground ring on socket card
LG - Ground ring on load card
DG - Ground terminal of DUT
DT - Any DUT terminal
SGG - Sector card ground

L1 - Load Relay No. 1 closed
L2 - Load Relay No. 2 closed
C5 - Comparator on the 5V range
C30 - Comparator on the 30V range
O - Sector connected as an output
I - Sector connected as an input

[2/] Typical paths are not considered unless so labeled.

a) TOP VIEW



1. SOCKET CARD GROUND RING
2. DECOUPLING CAPACITOR
3. HARDWIRED GROUND CONNECTIONS

b) BOTTOM VIEW

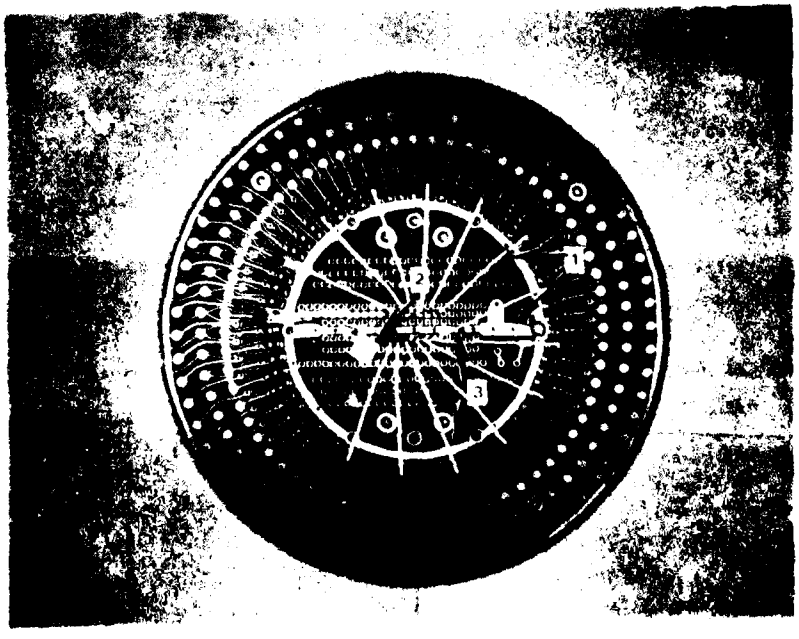


Figure 24. S3260 socket card with a 14-pin zero-insertion-force dual-in-line socket attached (approximately 1/2 scale)

defined in Section 3, was used to determine whether all DUTs would pass when 1 megohm was connected between all DUT terminals and ground. All of the TTL parts passed, and V_{IC} and I_{IH} values did not change. CMOS devices failed leakage current tests because of current flow through the added resistance, but timing parameters did not change. Since measurements of input leakage currents of less than 1 nanoamp must be made on CMOS devices with a forcing voltage of 15 volts, an open must be defined such that the leakage current through the open is at least 50 times less than the 1 nanoamp limit. This requires a resistance of more than 15 gigohms during measurement. An acceptable open condition for a CMOS input could be defined as "open ≤50 pf (a measurement system limitation) and $\geq 10^{10}$ ohm." For the bipolar and CMOS devices, a definition for the output condition as "open ≤50 pf and ≥1 megohm" would be adequate.

Ground path inductance and resistance were increased by removing the capacitor from its position between V_{CC} and the DUT ground terminals, and placing it between the V_{CC} terminal and the ground ring of the socket card. The hardwired ground connection was then removed and the ground terminal was connected both to the I- and the O-connection of the socket card, and then grounded through reeds in an S-3260 driver. This path represents 234 nanohenries of supply path inductance. Timing measurements were affected as shown in Table 21. The data indicate that any additional inductance can affect measurements noticeably.

Specifying a maximum acceptable inductance in a ground path is very difficult. Since the current in an inductor cannot change instantaneously, the switching current transients require time to dissipate. Higher inductance results in longer time delays. ATE using device handlers to speed through-put may be very hard pressed to meet a 50 nanohenry or 100 nanohenry requirement, yet the addition of less than 200 nanohenries produces considerable differences in timing parameters. A compromise definition of an adequate ground path could be "ground ≤ 200 nanohenries and ≤ 0.1 ohm." Although these suggested values would not lead to a guarantee of data reproducible to 3 percent accuracy, as was shown in Table 21, they do recognize the limitations of ATE and could be met with careful fixturing

on a variety of test systems. Further, any device meeting test requirements on a 200 nanohenry system would meet the requirements of a system furnishing a lower inductance ground path.

TABLE 21. PROPAGATION DELAY TIMES FOR TWO GROUND PATH INDUCTANCES

54LS295 Parameter	At 50 nH (ns)	At 234 nH (ns)	Percent Difference
t_{PHL}, data mode	29.4	31.4	6.5
t_{PHL}, serial mode	28.3	29.0	2.5
t_{PLH}, data mode	25.1	25.0	-0.2
t_{PLH}, serial mode	24.3	24.3	0.0
t_{ZL}	22.6	24.4	8.0
t_{LZ}	37.6	33.8	-10.0

15. SLASH SHEET REVIEW

During the course of the investigations previously described, the MIL-M-38510 slash sheets for each of the 13 device types were studied in detail to identify typographical errors, errors of omission, implied measurement conditions, redundant or superfluous measurements, and any errors or ambiguities in the notes and figures. Table 22 lists the revision and amendment of each slash sheet used for this study. Table 23 lists each of the items identified and their location in the specifications.

TABLE 22. PROCUREMENT SPECIFICATIONS USED DURING THIS STUDY

Generic Part Number	MIL-M-38510 Slash Number	Device Type	Revision	Amendment Number	Updated Through
5400	001	04	B	3	28 Jun 1976
5474	002	05	E	4	25 Jul 1978
54164	009	03	C	5	7 Jul 1978
54H74	022	03	B	1	1 Oct 1976
54H00	023	04	A	4	1 Jun 1977
4011A	050	01	C	-	16 Nov 1977
4013A	051	01	B	2	10 Sep 1976
4015A	057	03	B	2	7 Nov 1978
54S00	070	01	-	4	5 Apr 1978
54S74	071	01	A	3	19 Apr 1979
54LS00	300	01	A	2	14 Nov 1977
54LS74	301	01	A	1	18 Apr 1978
54LS295	306	06	B	1	12 Jun 1979

TABLE 23. IDENTIFICATION AND LOCATION OF SPECIFICATION ERRORS

Discussion Item	Listing of Occurrences	Comments
Additional conditions for I_{OS} measurements	/001, pp. 15, 17, 19, 21, 23 /002, pp. 38, 41, 45, 48, 52, 55, 59 /009, pp. 62, 65, 69, 74, 79, 83 /022, pp. 47, 50, 54, 58, 62, 64 /023, pp. 14, 17, 19, 21 /071, pp. 39, 47, 51, 55, 58, 59 /300, pp. 35, 40, 44, 50, 55 /301, pp. 76, 80, 85, 88, 92, 96, 100, 105 /306, pp. 60, 65, 69, 73, 76, 81, 85 Also MIL-STD-883B Test Method 3011	
Minimum or Maximum Recommended Pulse Widths	/009, p. 3	
Output Loading in Figures for Measurement of Time	/009, pp. 43, 46, 49, 55, 58 /057, pp. 31, 32, 35, 37 /306, pp. 27, 29, 32, 35, 38, 41, 44, 48	/009 p. 49 shows remaining outputs shorted /057 - The method used in these drawings is better than that used in the drawings for /009 or /306
Comparator levels for truth table tests	/002, pp. 39, 43, 46, 50, 54, 57, 61 /009, pp. 63, 67, 72, 77, 81, 84 /022, pp. 48, 52, 56, 60, 63, 67 /071, pp. 42, 46, 50, 54, 57, 61 /301, pp. 78, 82, 86, 90, 94, 98, 102, 107 /306, pp. 62, 67, 71, 75, 79, 89	

Table 23. Identification and Location of Specification Errors - continued

Discussion Item	Listing of Occurrences	Comments
50 Percent Duty Cycle	/001, p. 12 /002, pp. 21, 22, 23 /022, pp. 28, 29, 31, 32 /023, p. 11	
F_{MAX}, F_{CL} Limits Figures, conditions	/002, pp. 31, 33 /022, pp. 38, 39	
A. Figures and notes	/051, pp. 21, 23, 24, 27, 29 /057, pp. 31, 32, 34, 36, 38, 40 /071, p. 28	"observing proper output state changes"
B. Table III and notes	/002*, pp. 39, 42, 43, 46, 49, 50, 52, 53, 54, 57, 60, 61 /022*, pp. 5, 47, 48, 50, 51, 54, 58, 59, 62, 63, 65, 67 /051, pp. 34, 40 /057, pp. 44, 49, 54, 59, 64, 72 /071, pp. 40, 41, 42, 45, 46, 48, 50, 52, 54, 56, 57, 59, 61 /301, pp. 77, 78, 81, 82, 85, 86, 89, 90, 93, 94, 97, 98, 101, 102, 106, 107 /306, pp. 61, 62, 66, 67, 70, 71, 74, 75, 78, 79, 82, 83, 86, 88, 89	*Was correct in the table until amended to be incorrect
Flip-flop propagation delays	/002 /022 /071 /301	Occurs in Table III of each specification in subgroup 9, 10, and 11 testing

Table 23. Identification and Location of Specification Errors - continued

Discussion Item	Listing of Occurrences	Comments
Redundant or Omitted Measurements		
A. I_{SS}	/050, pp. 8	Only this case was examined. Other similar cases probably exist in this and most other CMOS specifications
B. Truth table testing	All subgroup 7 or 8 testing in the specifications	
C. Redundant f_{max} testing	/022, pp. 47, 48, 50, 51, 54, 55, 58, 59, 62, 63, 65, 66	
D. Insufficient f_{max} testing	300, pp. 61, 66, 70, 74 78, 81, 86	
Miscellaneous Errors and Omissions		Detailed in this report, Section 15, "TYPOGRAPHICAL ERRORS AND OMISSIONS"

ADDITIONAL CONDITIONS FOR I_{OS} MEASUREMENTS

Most manufacturers' data sheets specify that I_{OS} shall be measured with only one output grounded at a time and that no output be grounded for more than 1 second for most devices, or for more than 100 ms for some device types. Without such limitations, the device may dissipate much more power than it was designed to handle, and junction temperatures in excess of 200°C can quickly be reached. This problem has been recognized in the specification under paragraph 1.2.4. "Absolute maximum ratings," where, as Figure 25 shows, note 1 indicates that the device "Must withstand the added P_D due to short circuit conditions (e.g., I_{OS}) at one output for 5 seconds." As can be seen in Figure 26, note 4 to Table I of MIL-M-38510/002 adds, "Not more than one output should be shorted at a time."

However, devices are tested to the conditions of Table III, which has no notes limiting the test duration or requiring that the other outputs not be grounded (Figure 27). This specification may be technically correct since the absolute maximum ratings are not to be exceeded during test, and grounding more than one output would cause a power dissipation beyond the absolute maximum rating. However, it is not obvious from Table III that the specification prohibits this practice.

Since these limitations concern the method of measuring I_{OS}, MIL-STD-883B, Method 3011 should be modified to correct the situation. This can be done by an addition to Method 3011.1, paragraph 3, which currently reads

> The device shall be stabilized at the specified test temperature. Each output per package shall be tested individually.

The suggested addition is

> Output terminals not under test shall be open. Output terminals shall not be forced to the test condition voltage potential for a period longer than 5 seconds.

MIL-M-38510/2E
24 December 1974
SUPERSEDING
MIL-M-0038510/2D(USAF)
15 October 1973 and
MIL-M-38510/2C
7 November 1972

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, TTL, FLIP-FLOPS, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, bistable logic microcircuits. Three product assurance classes and a choice of case outline lead finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The complete part number shall be as shown in the following example:

M38510	002	01	B	A	C
Military designator	Detail specification	Device type (1.2.1)	Device class (1.2.2)	Case outline (1.2.3)	Lead finish (3.3)

1.2.1 Device type. Device type shall be as shown in the following:

Device type	Circuit
01	Single J-K master-slave flip-flop
02	Dual J-K master-slave flip-flop, no preset
03	Dual J-K master-slave flip-flop, no preset
04	Dual J-K master-slave flip-flop
05	Dual D-type edge-triggered flip-flop
06	Single edge-triggered J-K flip-flop
07	Dual D-type edge-triggered flip-flop, buffered output

1.2.2 Device class. Device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Letter	Case outline, MIL-M-38510, appendix C
A	F-1 (14-pin, 1/4" x 1/4", flat pack)
B	F-3 (14-pin, 1/8" x 1/4", flat pack)
C	D-1 (14-pin, 1/4" x 3/4", dual-in-line)
D	F-2 (14-pin, 1/4" x 3/8", flat pack)
E	D-2 (16-pin, 1/4" x 7/8", dual-in-line)
F	F-5 (16-pin, 1/4" x 3/8", flat pack)

1.2.4 Absolute maximum ratings.

Supply voltage range	-0.5 to 7.0 Vdc
Input voltage range	-1.5 Vdc at -12 mA to 5.5 Vdc
Storage temperature range	-65° C to 150° C
Maximum power dissipation per flip-flop, P_D	110 mW [1]
Lead temperature (soldering, 10 seconds)	300° C
Thermal resistance, junction to case, θ_{JC}	0.09° C/mW for flat packs 0.08° C/mW for dual-in-line pack
Junction temperature	T_J 175° C

[1] Must withstand the added P_D due to short circuit condition (e.g. I_{OS}) at one output for 5 seconds duration.

Figure 25. Page 1 of MIL-M-38510/2E showing that the absolute maximum ratings of the device types require withstanding an I_{OS} condition at only one pin for 5 seconds.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 9	Device type	Limits Min	Limits Max	Units
High-level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = 400 µA	All	2.4	---	Volts
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 16 mA	All		0.4	Volts
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{OL} = 12 mA, T_A = 25°C	All		-1.5	Volts
Low-level input current	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V 1	01, 02, 03, 04, 05, 06	-0.7	-1.6	mA
			07	-0.5	-1.6	mA
Low-level input current	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V 2	01, 02, 03, 04, 05	-1.4	-3.2	mA
			07	-1.0	-3.2	mA
Low-level input current	I_{IL3}	V_{CC} = 5.5 V, V_{IN} = 0.4 V 6	01, 02, 03, 04	-0.7	-3.2	mA
High-level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V 5	All	0	40	µA
High-level input current	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V 5	All	0	100	µA
High-level input current	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.4 V 3	All	0	80	µA
High-level input current	I_{IH4}	V_{CC} = 5.5 V, V_{IN} = 5.5 V 3 7	All	0	200	µA
High-level input current	I_{IH5}	V_{CC} = 5.5 V, V_{IN} = 2.4 V 7 8	01, 02, 03, 04, 05, 07	-850	-50	µA
				0	120	µA
High-level input current	I_{IH6}	V_{CC} = 5.5 V, V_{IN} = 5.5 V 8	05, 07	0	300	µA
Short-circuit input current	I_{OS}	V_{CC} = 5.5 V, V_{IN} = 0 V 4	All	-20	-57	mA
Supply current per device	I_{CC}	V_{CC} = 5.5 V, V_{IN} = 5 V	01		20	mA
			02, 03, 04		40	
			05, 06, 07		30	
Maximum clock frequency	f_{MAX}		01, 02, 03, 04, 05, 07	5		MHz
			06	4.5		
Propagation delay to high logic level (clear or preset to output)	t_{PLH}		01, 02, 03, 04, 05	5	39	ns
			06	5	62	
			07	5	31	
Propagation delay to low logic level (clear or preset to output)	t_{PHL}	V_{CC} = 5 V, CL = 50 pF minimum, RL = 390 Ω ±5%	01, 02, 03, 04, 05	5	50	ns
			06	5	62	
			07	5	39	
Propagation delay to high logic level (clock to output)	t_{PLH}		06	5	62	ns
			01, 02, 03, 04, 05	5	39	
			07	5	31	
Propagation delay to low logic level (clock to output)	t_{PHL}		06	5	62	ns
			01, 02, 03, 04, 05	5	50	
			07	5	39	

1 Input condition - J or K for device types 01, 02, 03, 04, 06, and preset or D for device types 05 and 07, and clock, clear or preset for device type 06.
2 Input condition - Clock for device types 01, 02, 03 and 04, and clear or clock for device types 05 and 07.
3 Input condition - Clear or preset for device types 01, 02, 03, 04, 05, 06 and 07 and clock for device types 05 and 07.
4 Not more than one output should be shorted at a time.
5 Input condition - J or K for device types 01, 02, 03, 04, 06, and D for device types 05 and 07, and clock for device type 06.
6 Input condition - Clear or preset for device types 01, 02, 03 and 04.
7 Input condition - [illegible] for device types 01, 02, 03, and 04.
8 Input condition - [illegible] for device types [illegible] and [illegible].
9 See table III [illegible] for device type [illegible].

Figure 26. MIL-M-38510/2E, page 3, Table I, Note 4 requires that no more than one output be shorted at one time.

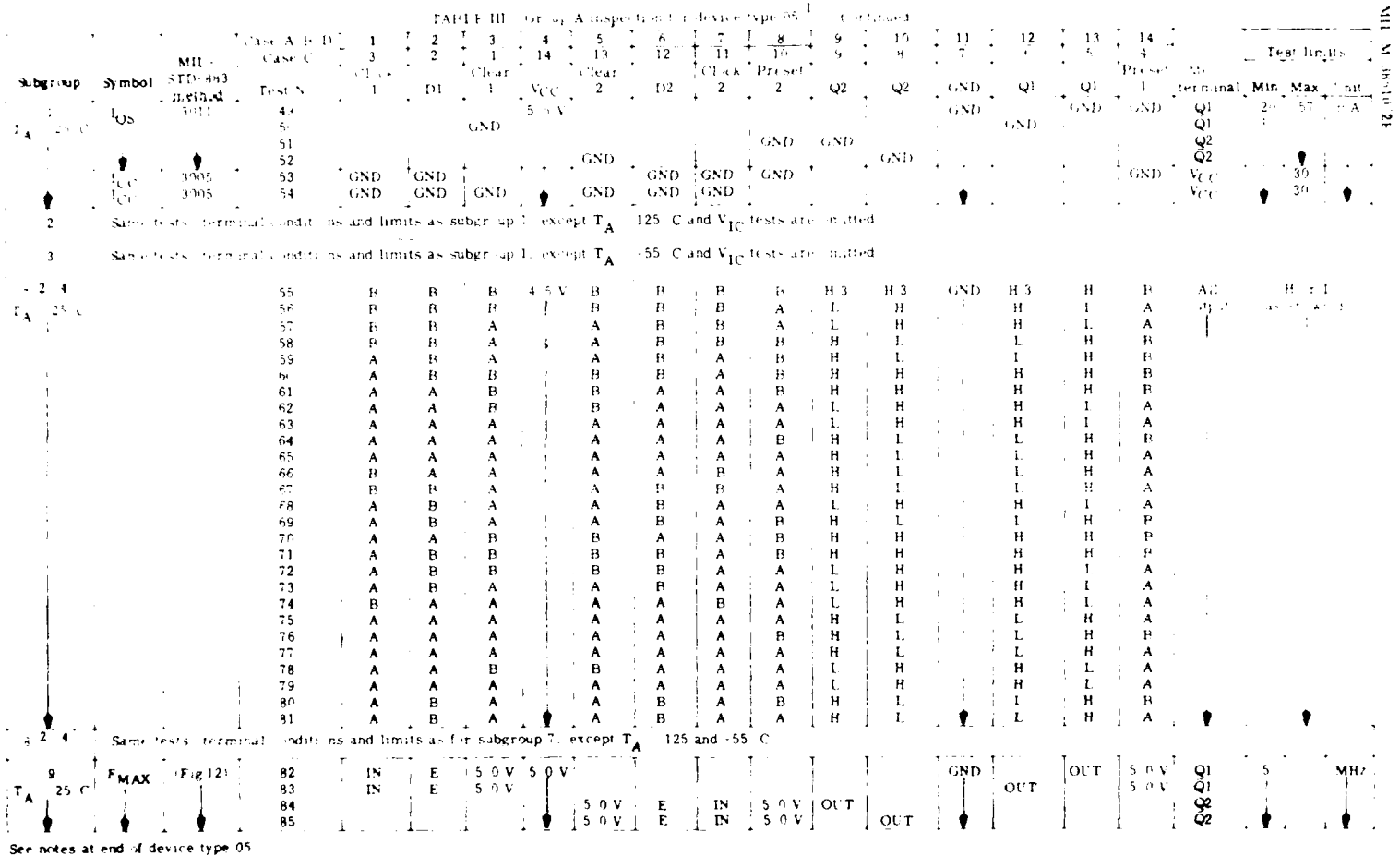


Figure 27. MIL-M-38510/2E, no maximum duration specified for I_{OS} and no restriction placed on untested outputs (no notes apply).

MINIMUM OR MAXIMUM PULSE WIDTH IN RECOMMENDED OPERATING CONDITIONS IN MIL-M-38510/9C.

Page 3 of MIL-M-38510/9C presents some confusing recommended operating conditions for device types 02 and 03 (Figure 28). The specification recommends operating the 02 device with a minimum clock pulse width of 35 nanoseconds maximum. Does this imply that operation with a clock pulse width less than 35 nanoseconds is recommended? No. What was intended was that no device should fail to perform with a clock pulse width of 35 nanoseconds, which is a worst case or maximum acceptable minimum clock pulse width. This can be stated more clearly simply by declaring that the recommended width of the clock pulse be 35ns minimum, as was done for device type 05 on the same page of the specification. An alternative approach is to delete the words maximum and minimum following the recommended limit value as was done in MIL-M-38510/306B, p. 2 (Figure 29).

OUTPUT LOADING IN FIGURES FOR MEASUREMENTS OF TIME

When several outputs require similarly constructed loads, as on p. 55 of MIL-M-38510/9C (Figure 30), the notation "same output load as output A" is used to avoid drawing a number of loads unnecessarily. However, the wording chosen leaves open the possibility of connecting the same load to all the outputs (shorting the outputs together) or connecting the same single load to each of the outputs in turn. This ambiguity can be avoided by changing the wording to "output load configured as load of output A."

COMPARATOR LEVELS FOR TRUTH TABLE TESTS

The specifications allow either of two methods to be used to determine whether proper output states are observed during truth table tests (subgroups 7 and 8). As can be seen in note 4 of Figure 31, a high can be

Device type 02

Minimum clock pulse width	35 ns	maximum
Minimum clear pulse width	30 ns	maximum
Minimum preset pulse width	30 ns	maximum
Serial input setup time	30 ns	minimum
Serial input hold time	0 ns	minimum

Device type 03

Minimum clock pulse width	30 ns	maximum
Minimum clear pulse width	50 ns	maximum
Serial setup time	15 ns	minimum
Serial hold time	10 ns	maximum

Device type 04

Width of clock input pulse	25 ns	minimum
Width of load input pulse	15 ns	minimum
Clock enable setup time	30 ns	minimum
Parallel input setup time	10 ns	minimum
Serial input setup time	20 ns	minimum
Shift setup time	45 ns	minimum
Hold time at any input	10 ns	maximum

Device type 05

Width of clock input pulse	20 ns	minimum
Width of clear input pulse	20 ns	minimum
Data input setup time	20 ns	minimum
Clear input setup time	25 ns	minimum
Hold time at any input	0 ns	minimum
Mode control setup time	30 ns	minimum

Device type 06

Width of clock input pulse	16 ns	minimum
Width of clear input pulse	12 ns	minimum
Shift load input setup time	27 ns	minimum
Data input setup time	20 ns	minimum
Clear input setup time	25 ns	minimum
Shift load release time	10 ns	maximum
Data hold time	0 ns	minimum

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

Figure 28. MIL-M-38510/9C, page 3.

1.3 Absolute maximum ratings.

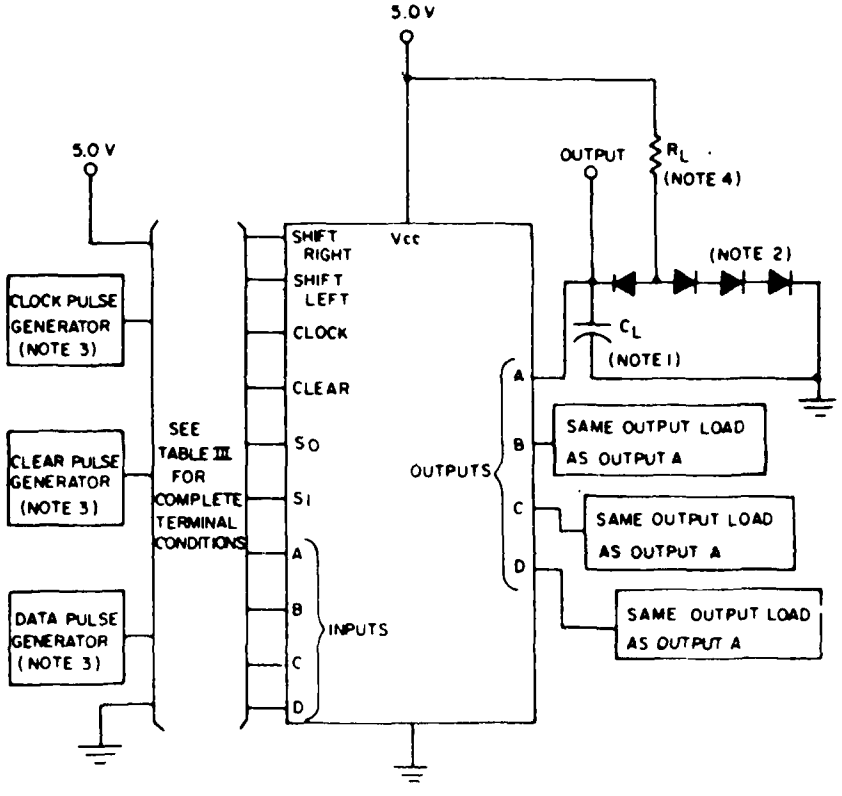
Supply voltage range	-0.5 Vdc to 7.0 Vdc
Input voltage range	-1.5 Vdc at -18 mAdc to 5.5 Vdc
Storage temperature range	-65°C to 150°C
Maximum power dissipation per register, P_D 1/	
Device type 01	127 mWdc
Device type 02, 03	116 mWdc
Device type 04	110 mWdc
Device type 05	149 mWdc
Device type 06, 07	160 mWdc
Device type 08	198 mWdc
Device type 09	209 mWdc
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance (junction to case)	θ_{JC} = { 0.09°C/mW for flat pack; 0.08°C/mW for dual-in-line pack
Junction temperature	T_J = +175°C

1.4 Recommended operating conditions.

Supply voltage	4.5 Vdc minimum to 5.5 Vdc maximum
Minimum high level input voltage	2.0 Vdc
Maximum low level input voltage	0.7 Vdc
Ambient operating temperature range	-55°C to 125°C
Minimum clock pulse width:	
Device type 01, 03, 05, 07, 09	20 ns
Device type 02	18 ns
Device type 04, 06, 08	25 ns
Minimum clear pulse width:	
Device type 01, 05, 09	20 ns
Device type 02	15 ns
Device type 04	30 ns
Device type 07	25 ns
Minimum load pulse width:	
Device type 08	15 ns
Minimum setup time at mode control:	
Device type 01	30 ns
Device type 03, 06	20 ns
Minimum setup time at shift/load:	
Device type 02	25 ns
Device type 07	20 ns
Device type 08	45 ns
Device type 09	30 ns
Minimum setup time at serial data:	
Device type 08	10 ns
Minimum setup time at serial or parallel data:	
Device type 01, 02, 03, 05, 06, 07, 09	20 ns
Device type 04	30 ns
Minimum setup time at preset:	
Device type 04	30 ns
Minimum setup time at inhibit:	
Device type 08	30 ns
Minimum hold time:	
Device type 01, 02, 03, 04, 05, 07	10 ns
Device type 06	20 ns
Device type 08, 09	0 ns
Minimum enable or inhibit time of clock :	
Device type 03	20 ns
Maximum release time of shift/load:	
Device type 02	10 ns

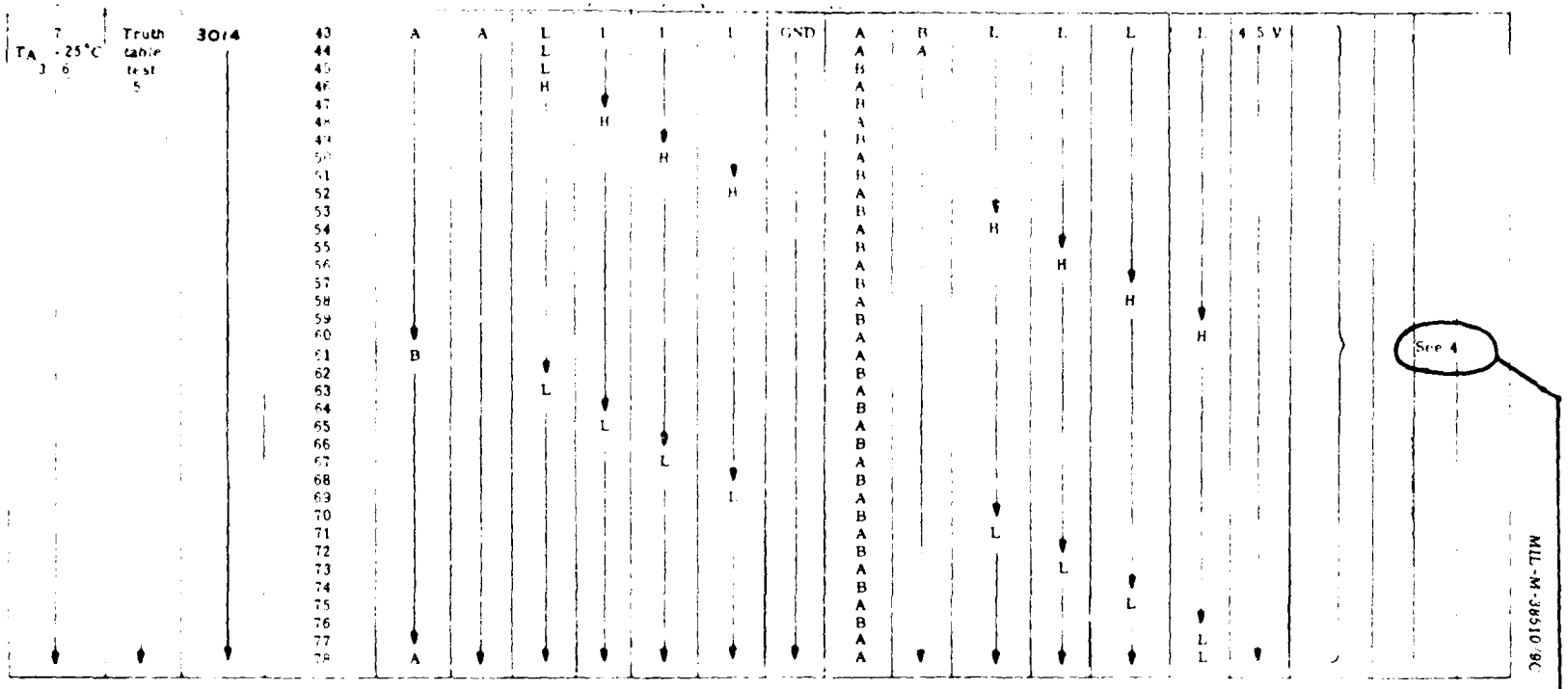
1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

Figure 29. MIL-M-38510/306B, page 2.



NOTES:
1. C_L = 50 pF minimum including probe and jig capacitance.
2. All diodes are 1N3064, or equivalent.
3. Unless otherwise specified in the notes associated with the individual tests, all pulse generators have the following characteristics: Z_{OUT} = 50Ω, $t_{TLH} \leq$ 7 ns, $t_{THL} \leq$ 7 ns, V_{IH} = 3.0 V minimum, V_{IL} = 0.
4. R_L = 400Ω ±5%.

Figure 30. From MIL-M-38510/9C, page 55.



See footnotes at end of device type 03

1 A = normal clock pulse except for subgroups 7 and 8 (see 3.)
2 B = momentary GND then 4.5 V to clear register prior to test, except for subgroups 7 and 8 (see 3.)
3 For subgroups 7 and 8, A = V_{CC} and B = GND.
4 Output voltages shall be either
(a) H = 2.4 V minimum and L = 0.4 V maximum when using a high speed checker double comparator, or
(b) H = 1.5 V and L = 1.5 V when using a high speed checker single comparator.
5 The tests in subgroups 7 and 8 shall be performed in the sequence specified.
6 Only a summary of attributes data is required.
7 For device type 03, with schematics incorporating 4 kΩ base resistors, the minimum and maximum limits shall be -0.7 and -1.6 mA, respectively.
For schematics incorporating 6 kΩ base resistors, the minimum and maximum limits shall be -0.4 and -1.3 mA, respectively.
8 For device type 03 with schematics incorporating a 4 kΩ base resistor in the clear input circuit, the minimum and maximum limits shall be -1.4 and -3.2 mA, respectively.
For schematics incorporating 6 kΩ base resistors in the clear input circuit, the minimum and maximum limits shall be -0.8 and -2.6 mA, respectively.

Figure 31. From MIL-M-38510/9C, pages 69 and 72. Two different sets of comparator levels are permitted.

measured as either 2.4V minimum or as 1.5V minimum and a low as 0.4V maximum or as 1.5V maximum. This allows two measurement standards, one less severe than the other, with the possibility of passing devices using one standard and failing them using the other. If the less severe measurement technique is acceptable, then there is no need for the more severe alternative. If the less severe technique is not acceptable, then it should be eliminated. Further discussion is withheld for the section on redundant measurements.

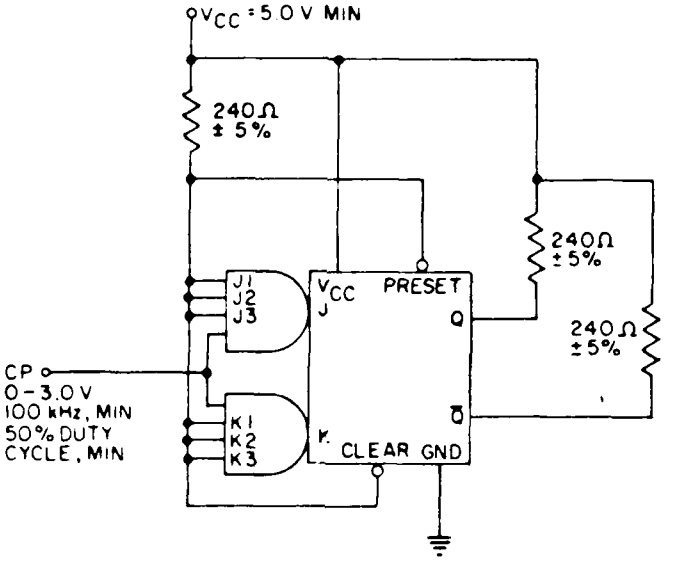
FIFTY PERCENT DUTY CYCLES

The burn-in circuits for MIL-M-38510/22B specify a clock pulse with a "50 percent DUTY CYCLE, MIN" as shown in Figure 32. This permits a clock pulse of 99 percent duty cycle or one of 50 percent. A 99-percent duty cycle does not exercise the device any better than a 1-percent duty cycle. The clock pulse generator would be better specified as having a "50 percent duty cycle ± 10 percent" or a "50 to 60 percent duty cycle." This was done in MIL-M-38510/301A on pages 57 to 60.

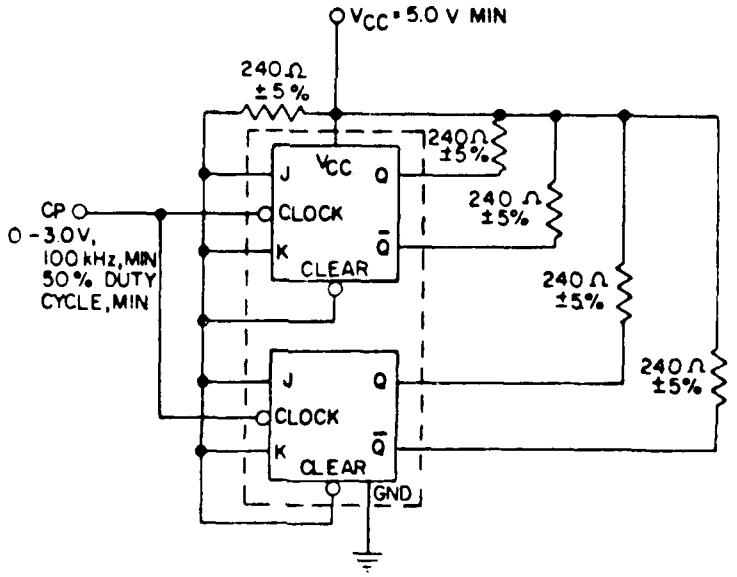
F_{MAX} LIMITS AND TEST CONDITIONS

Several inconsistencies in MIL-M-38510 tests for f_{MAX} were noted in the /9, /22, and /71 specifications. Other inconsistencies are found in Table III.

The test circuit of page 38 of MIL-M-38510/22B is not correct for f_{MAX} since the $\overline{Q}$ output is not connected to the D input as called out in Table III (Figure 33). Also, such a connection would load $\overline{Q}$, and the external load either should be adjusted to compensate or be eliminated. The voltage waveforms for the D input are not correct for f_{MAX} either, as t_1, t_0, t_{setup}, and t_{hold} are controlled by the characteristics of the $\overline{Q}$ output and not by a programmable pulse generator. Each of these problems would be most easily addressed by using a separate figure for f_{MAX}, thus avoiding confusion between f_{MAX} conditions and conditions required for propagation delay time measurements. This was done in parts of MIL-M-38510/9C (e.g., page 47). Note that connecting the input of a



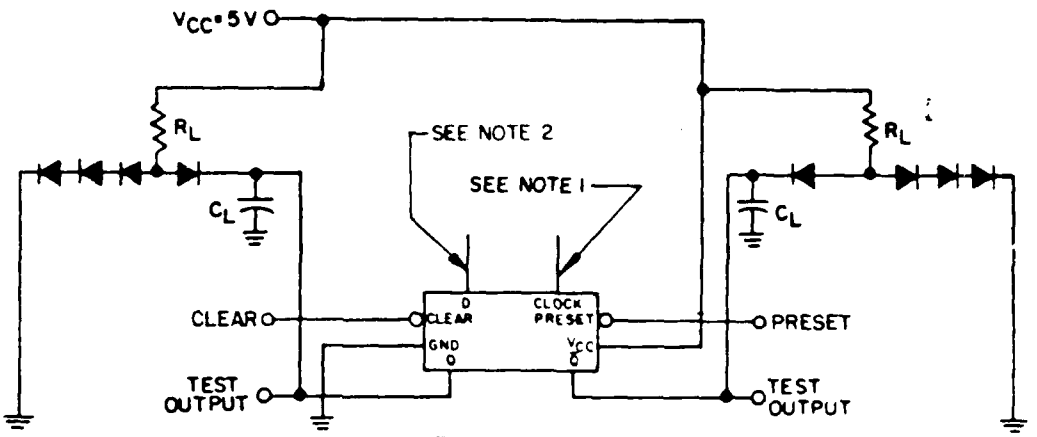
Device type 01



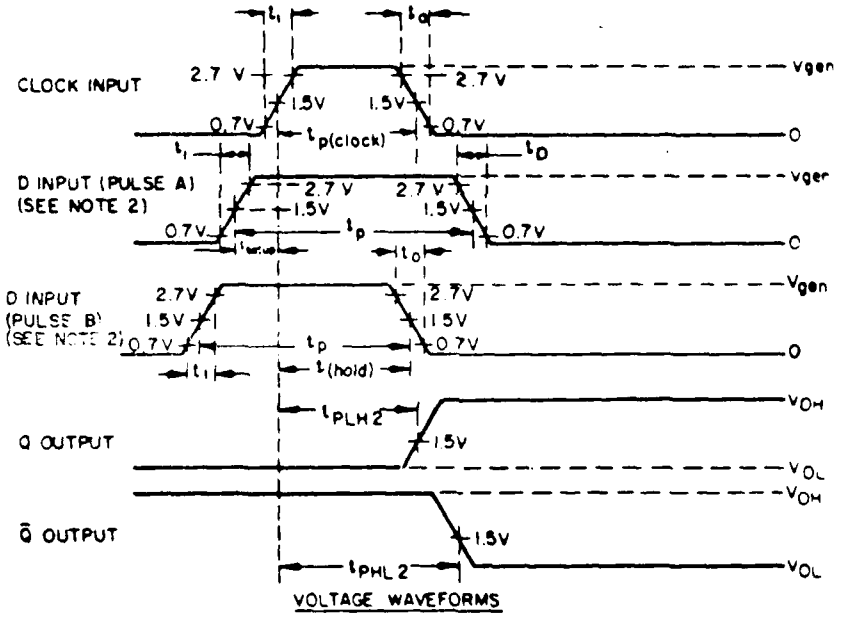
Device type 02

FIGURE 4. Burn-in and life-test circuits.

Figure 32. MIL-M-38510/22B, page 28, clock pulse specified as having "50 percent DUTY CYCLE, MIN."



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

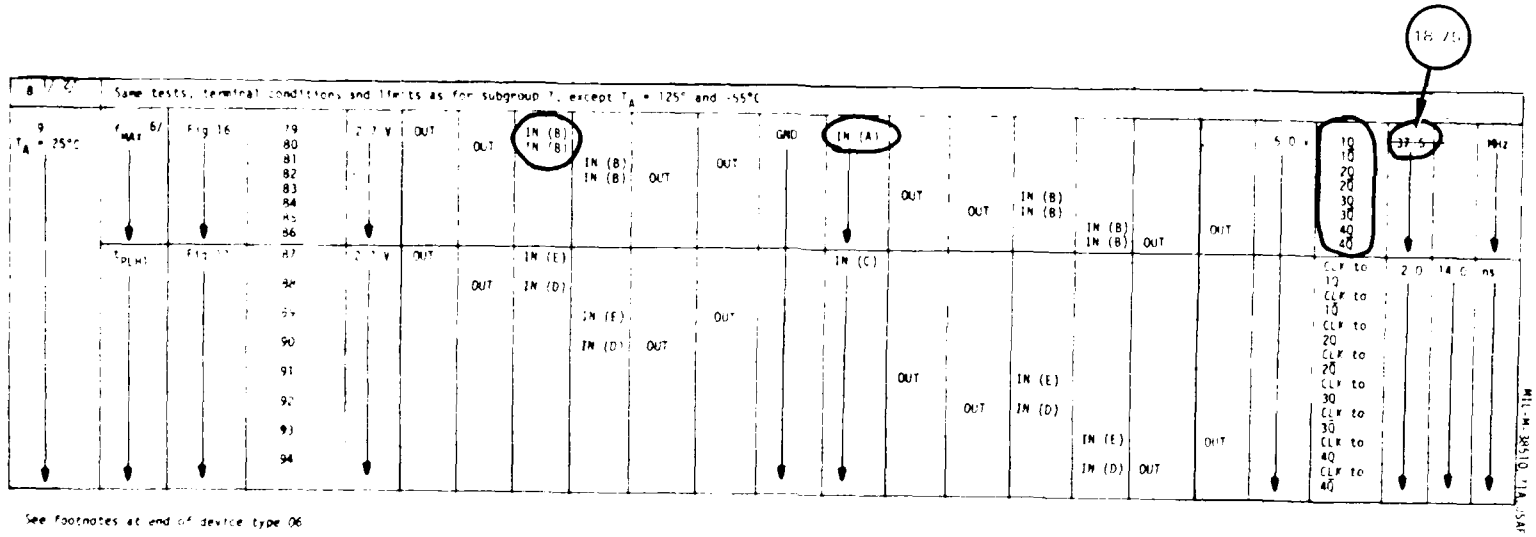
1. Clock input pulse has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 7$ ns, $t_{p(clock)}$ = 20 ns, and PRR = 1 MHz. When testing f_{MAX}, f = 36 MHz for subgroup 9 and f = 28 MHz for subgroups 10 and 11.
2. D input (pulse A) has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 7$ ns, t_{setup} = 10 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics. V_{gen} = 3 V, $t_0 = t_1 \leq 7$ ns, t_{hold} = 5 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ±5% (including jig and probe capacitance).
5. R_L = 280Ω ±5%.

Figure 33. MIL-M-38510/22B, page 38, f_{MAX} test conditions conflict with other switching test conditions.

flip-flop to the $\overline{Q}$ output is inconvenient on ATE, often requiring special fixturing and a connector length which adds inductance to the connection. This, in addition to the inability of ATE to run at clock rates in excess of 20 or 25 megahertz, is a reason to desire an alternative to the current f_{MAX} test method, as discussed in Section 13. The MIL-M-38510/301A method of testing f_{MAX} which uses a pulse generator on the D input instead of connecting $\overline{Q}$ to D is much easier to implement on ATE and should be considered as a replacement for the method used in MIL-M-38510/9, /22, and /71.

The remaining inconsistencies are found in the various Table III entries pertaining to f_{MAX} for TTL or f_{CL} for CMOS devices. Referring to Figure 34, the f_{MAX} limit applies to the clock input frequency, yet the measured terminals are the outputs. Even though this is explained in note 6, it is inconsistent to measure at a Q terminal to a limit which does not apply at that terminal. Further, note 6 states that the output frequency shall be one-half of the input frequency. IN(A) and IN(B) use two different pulse repetition rates (PRR). Of which is the output one-half? In the flip-flops which require the $\overline{Q}$ output be connected to the D input, is the output PRR required to be one-half of itself? Clearly this is not what is intended. These inconsistencies can be resolved by making the measurement limit the desired output PRR and specifying that the higher input PRR be applied in the value for f_{MAX} at the clock input.

Figure 35 is page 40 of 51B. Note "O" reads, "The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur..." but "proper output state changes" are not defined in Table III. If an unusual wave shape results from the test, who determines whether the output state changes are proper? The phrase "...if the output state changes according to figure 2..." would be more precise because the truth tables of figure 2 define the proper output state changes, and note "N" defines the required output signal levels.



NOTES

1. [illegible] of all device data is required.
2. [illegible] shall be A 2.0 Volts minimum and B 0.8 Volts maximum.
3. [illegible] shall be for H 2.4 V, minimum and L 0.4 V, maximum when using a high speed checker double comparator or [illegible] when using a high speed checker single comparator.
4. [illegible] pulse.
5. [illegible] from 5.0 V to momentary GND to 5.0 V occurs before measurement is made.
6. ~~[illegible] shall specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.~~
7. [illegible] specified is frequency of the output pulses. PRR for IN(A) shall be twice the output PRR.

Figure 54. Suggested revision for MIL-M-38510-71A, pages 59 and 61, f_{MAX} conditions and limits.

AD-A093 215 HUGHES AIRCRAFT CO CULVER CITY CA F/G 14/2
EVALUATION OF ELECTRICAL TEST CONDITIONS IN MIL-M-38510 SLASH S--ETC(U)
AUG 80 K SANDGREN F30602-78-C-0193
UNCLASSIFIED HAC-FR-80-76-706 RADC-TR-80-263 NL

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TABLE III. Group A inspection for device type 02. -Continued.

Symbol	MIL-STD-883 method	Cases E, F	Terminal conditions and limits																Measured terminal	Test limits						Units
																				Subgroup 9 T_A = 25°C		Subgroup 10 T_A = 125°C		Subgroup 11 T_A = -55°C		
		Symbol	Q_1	$\overline{Q}_1$	CLK_1	RS_1	K_1	J_1	SET_1	V_{SS}	SET_2	J_2	K_2	RS_2	CLK_2	$\overline{Q}_2$	Q_2	V_{DD}		Min	Max	Min	Max	Min	Max	
		Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16								
t_{SLH}	Fig 19	171								GND			IN		IN			5.0 V	K_2 to CLK_2		150		225		150	ns
		172										IN			IN			5.0 V	J_2 to CLK_2		150		225		150	ns
t_{RLH}		173	OUT		IN		IN												K_1 to CLK_1							
		174	OUT		IN			IN											J_1 to CLK_1							
		175											IN		IN		OUT		K_2 to CLK_2							
		176										IN			IN		OUT		J_2 to CLK_2							
t_{RHL}		177	OUT		IN		IN												K_1 to CLK_1							
		178	OUT		IN			IN											J_1 to CLK_1							
		179											IN		IN		OUT		K_2 to CLK_2							
		180										IN			IN				J_2 to CLK_2							

NOTES

A. Pins not designated may be "high" level logic, "low" level logic or open.
B. Test numbers 21 thru 34 shall be run in sequence.
C. I_{OH} = -0.25 mA at 25°C, -0.175 mA at 125°C, -0.31 mA at -55°C.
D. V_{IH1} = 3.8 V at 25°C, 3.6 V at 125°C, 3.95 V at -55°C.
E. V_{IH2} = 9.5 V at 25°C, 9.25 V at 125°C, 9.75 V at -55°C.
F. I_{OL} = 0.5 mA at 25°C, 0.35 mA at 125°C, 0.65 mA at -55°C.
G. V_{IL1} = 1.1 V at 25°C, 0.85 V at 125°C, 1.35 V at -55°C.
H. V_{IL2} = 2.8 V at 25°C, 2.55 V at 125°C, 3.05 V at -55°C.
I. For input voltage conditions see Figure 15.
J. For input voltage conditions see Figure 16.
K. The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.
L. See 4.4.1(c).
M. Test numbers 101 thru 117 shall be run in sequence and the functional tests shall be performed with V_{IH} and V_{DD} < 5.0 V and ≥ 15.0 V.
N. L = 0.5 V maximum and H = 4.5 minimum.
O. The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.
P. Pulse repetition period = 100 μ sec, 50 percent duty cycle. The maximum clock transition time (t_{TLHCL}) requirement is considered met if proper output state changes occur with the rise time set to that given in the limits column.
Q. The minimum clock pulse width (t_p) requirement is considered met if proper output state changes occur with the pulse width set to that given in the limits column.

MIL-M-38510/51B

Figure 35. MIL-M-38510/51B, page 40.

FLIP-FLOP PROPAGATION DELAY

MIL-M-38510 requirements for flip-flop propagation delay times were reviewed in detail during this investigation. Figure 36 is a logic diagram of a D-type flip-flop. Observe that the Q output is an input to the NAND gate providing the $\overline{Q}$ output and vice versa. This implies that Q cannot enter a low state until after $\overline{Q}$ enters a high state and that $\overline{Q}$ cannot enter a low state until Q enters a high state. Stated differently, T_{PHL} of one output is equal to T_{PLH} of the other output plus the delay of the final NAND gate. If a device passes T_{PHL} at Q it must have also passed T_{PLH} at $\overline{Q}$, since T_{PLH} at $\overline{Q}$ was an integral part of the measurement. The T_{PLH} measurements appear to be redundant and could be deleted without reducing the thoroughness of the Table III testing. However, if those tests were deleted and a T_{PHL} failure occurred, the failing portion of the device (output gate or input gate) would not be readily identifiable. Thus the T_{PLH} test data is useful in tracking reliability problems. It is not suggested that the T_{PLH} tests be deleted.

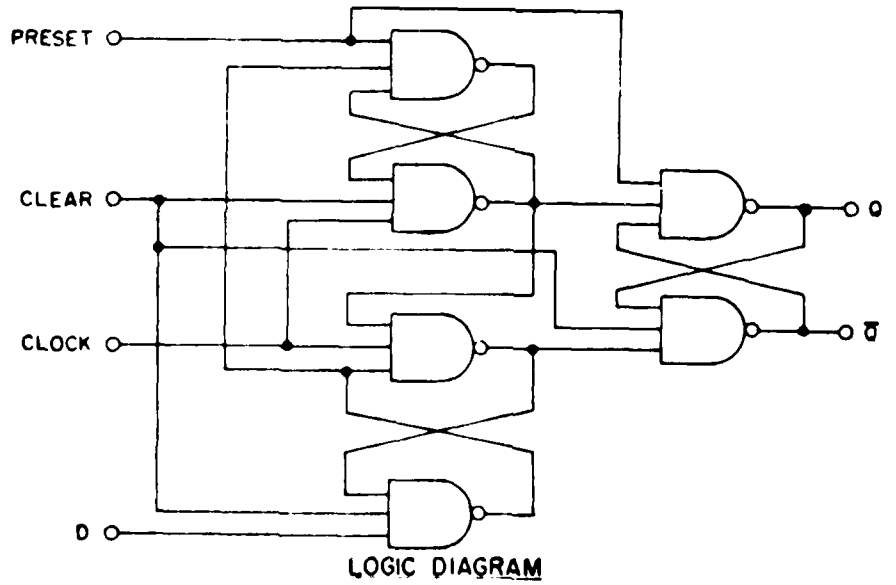

Figure 36. Logic diagram of a D-type flip-flop (from MIL-M-38510/22B, p. 17).

REDUNDANT OR SUPERFLUOUS MEASUREMENTS AND OMITTED MEASUREMENTS

While reviewing the MIL-M-38510 slash sheets, a number of tests were encountered that do not provide additional information and are therefore redundant. Among these tests are an I_{SS} test, truth table testing, and some f_{MAX} tests. In addition, an omitted measurement for some f_{MAX} tests is discussed.

FET Supply Current Tests

Test 18 of MIL-M-38510/50C, Table III for device type 01, shown in Figure 37 is redundant. As Figure 38 shows, the current I_{SS} consists of leakage from the input gates plus leakage from V_{DD} through the channels of the individual FETs. Tests 17 and 19 produce the two possible worst case conditions for leakage from V_{DD} by turning on either the P-channel or the N-channel FETs. Input leakage currents are measured separately as I_{IH} and I_{IL}. Considing the other I_{SS} and I_{IH} measurements, test 18 provides no new information and should be deleted.

Truth Table Testing

As was discussed in Section 8, truth table testing can give information about dynamic V_{IH} and V_{IL} and also can assure that the devices change state according to the truth table. The current specifications do not require input conditions yielding this $V_{IL_{max}}$ and $V_{IH_{min}}$ information. Assurance of operation according to a truth table could be provided by the subgroup 9 tests (f_{MAX} and propagation delay time measurements) if the preconditioning and test sequence were specified. Therefore, although the truth table tests (subgroups 7 and 8) could be eliminated as redundant, they should be retained but run with tighter limits on input conditions to provide additional information.

Testing for f_{MAX}

Four f_{MAX} tests are specified in Table III of MIL-M-38510/2E for device types 02, 03, 04, 05, and 07. A separate f_{MAX} test is specified for each output and each complemented output although the same set of input

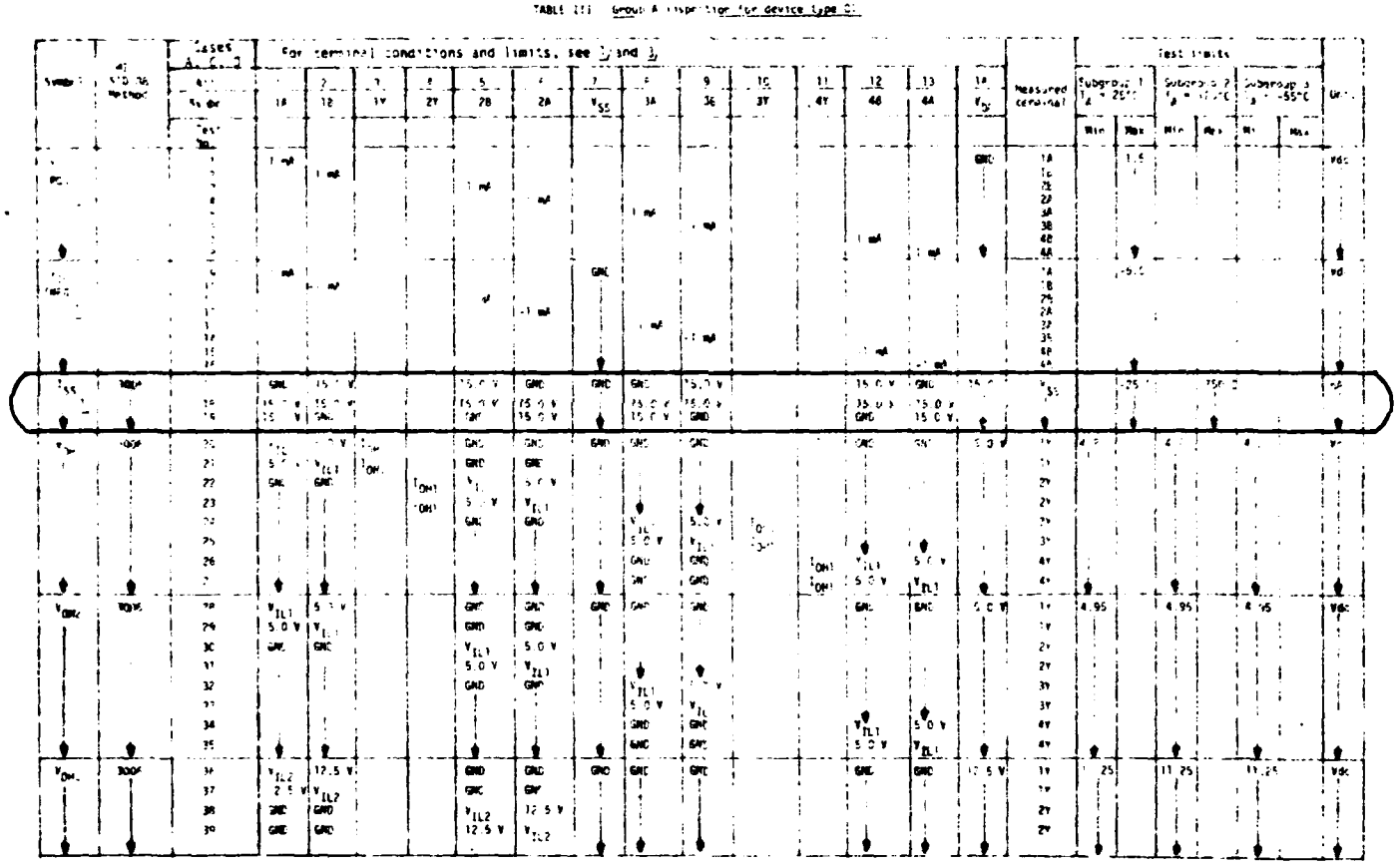

Figure 37. I_{SS} requirements for FET (from MIL-M-38510/50C, page 12).

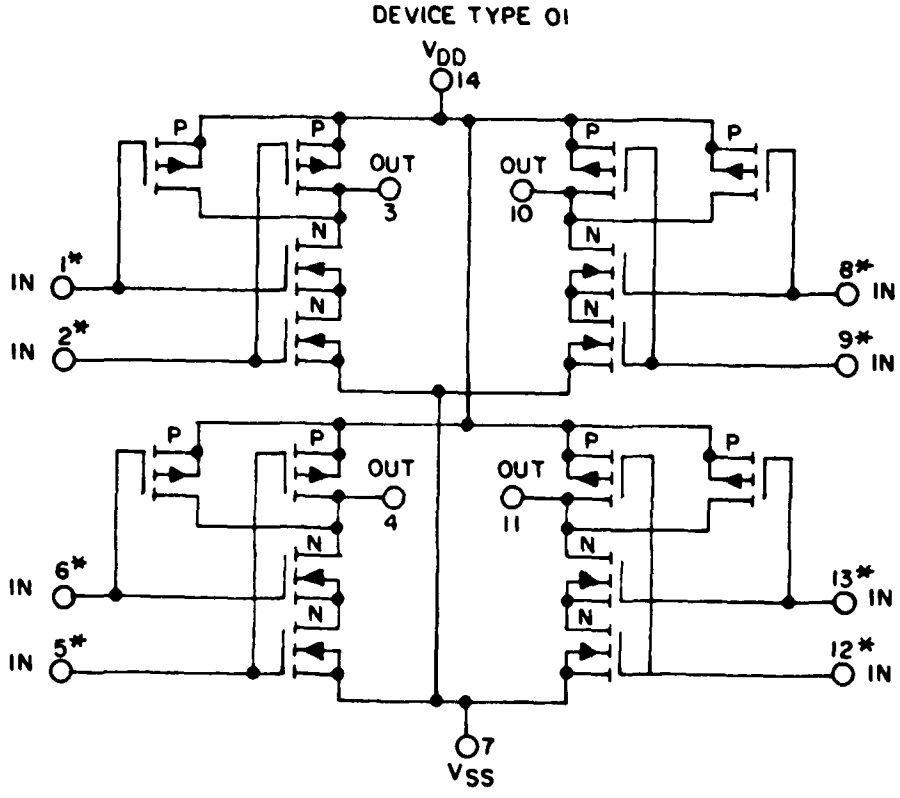

Figure 38. Schematic of CD4011A (MIL-M-38510/50C, p. 8).

conditions could be used for all four tests. In an age of multiple-trace oscilloscopes and ATE capable of testing all outputs simultaneously, one combined f_{MAX} test could replace the four currently specified. Even if this were not done, having demonstrated the interdependence of the Q and $\overline{Q}$ outputs and utilizing the propagation delay, V_{OH}, and V_{OL} measurements to demonstrate the capability of the output to drive a load, it has been determined that testing f_{MAX} on Q output is an adequate test of the $\overline{Q}$ output. Therefore, two of the four f_{MAX} tests may be deleted as redundant.

Omitted f_{MAX} Measurement Condition

In some multi-stage shift registers, the f_{MAX} test is performed at only one output. For example, in MIL-M-38510/306B, page 82, only Q_A of the 54LS295 is tested. Examination of Figure 39 shows that even if

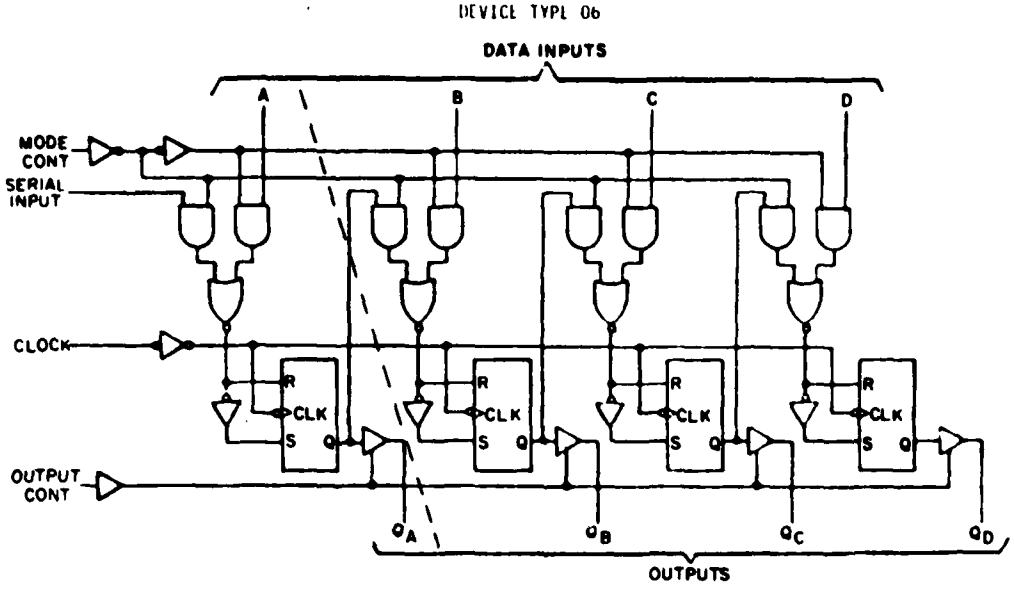

Figure 39. Logic diagram of 54LS295 (MIL-M-38510/306B, page 24).

the longest single stage delay path is from the serial input to the output Q_A, a proper square wave output at Q_A does not guarantee a proper output at Q_B, Q_C, or Q_D. A fault anywhere to the right of the dashed line would not be detected. As a minimum, Q_A and Q_D need to be tested. A fault in the output buffer gate at either Q_B or Q_C might still go undetected by the f_{MAX} test, since the following stage is connected before the buffer, but such faults would be detected in propagation delay tests.

Similarly, counters are sometimes tested for f_{MAX} at only the most rapidly varying stage, using the theory that no other stage has to switch at more than one-half the frequency of this stage. However, device design may take this into account, and the delay paths into subsequent stages may be sufficiently long that the second most rapidly varying stage may not meet the one-half f_{MAX} requirements. Also, signal levels within a device operated at f_{MAX} may not be sufficient to drive succeeding stages reliably. If outputs are buffered, the reduced signal level would not be apparent by any test other than f_{MAX} at both the most rapidly and least rapidly varying outputs.

TYPOGRAPHICAL ERRORS AND OMISSIONS

In addition to those ambiguous or incorrect situations previously described, the following are minor errors that were found.

Page No.	MIL-M-38510/2F
3	Note 4 reads "Nor more..." It should read "Not more..."
16	The note "Schematic shows one-half of dual unit" should be a note for all three drawings, not just circuit B, and should be placed under the notes heading of page 17.
	MIL-M-38510/9C
13-14	The function tables have neither a figure number, nor a table number, nor are they text. They should be labelled as part of figure 2 "Truth tables and timing diagrams."
41	Note reads "$R_2 = R_6 = 220\ \Omega \pm 10\%$." It should read "$R_2$ through $R_6 = 220\ \Omega \pm 10\%$" or "$R_2 = R_3 = R_4 = R_5 = R_6 = 220\Omega \pm 10\%$."
49	Figure 8 shows several outputs shorted together before being connected to loads. Since there is not adequate space to draw the load eight times, Q_B through Q_H should be separately connected to a single rectangle in which is inscribed "Connect each output with an output load configured as the load at output A."
	MIL-M-38510/22B
2	In note 2, the output fanout needs further definition. A type 06 output may not drive 10 type 06 clear or clock inputs at 150 μA each when high level current capability is only 0.5 mA. This can be corrected by restating note 2 as "Device will fanout in both high and low levels to the specified number of D, J, or K inputs of the same device type."
8	In the figure for terminal conditions of device type 02, the two K terminals, the two Q terminals, etc. need to be differentiated as K1 and K2, Q1 and Q2, etc.
31	In the figure, a current limiting resistor (240 ohm) would be appropriate between V_{CC} and the inputs.
34, 36, 38, 41, 43, 45	The notes say, "When testing f_{MAX}, f = ..." They should say, "When testing f_{MAX}, PRR = ..."

Page No.	MIL-M-38510/22B (continued)
55	The arrow in the max column under "22" extends to Test 105. It should stop at Test 101.
67 and following pages	If page 67 is the last page of the document, where is paragraph 6 and information about the preparing activity?
	MIL-M-38510/23A
9-10	Less confusion would arise if all versions of these circuits were drawn with the same number of inputs.
	MIL-M-38510/50C
4	Paragraph 4.4.1(e) reads: "Device input pins not designated in tests may be tied to V_{CC} or GND or may be open provided measurements are not affected. Device output pins not designated in tests may be loaded or open provided measurements are not affected." If measurements were to be affected, which condition would prevail? It is suggested that the following statement be added: "If measurements are found to be affected, input pins not designated in tests shall be tied to the voltage level that will yield a worst case measurement value, and output pins not designated shall be loaded.
7-8	Case dimensions are a part of the general specification MIL-M-38510D. Figure 1 is not required. The references to figure 1 should be changed to reference the appropriate figure in M38510D, Appendix C.
29	Paragraph 6.4. The symbols "t_f" and "t_r" are not used anywhere in this specification ("$t_{THL(1)}$" and "$t_{TLH(1)}$" are used), so reference to their use can be deleted.
	MIL-M-38510/71A
30	In note 1 the symbol "dc" is used for duty cycle. This symbol is more generally used for direct current. Duty cycle should be spelled out.
	MIL-M-38510/306B
58	The caption under the title reads "... oropen)", it should read "... or open)"

Page No.	MIL-M-38510/306B (continued)
83	Subgroup 11 is missing.
98	Paragraph 4.5.1 Voltage and current, which reads, "All voltages given are referenced to the ground terminal. Currents given are conventional current and position when flowing into the referenced terminal," would be better placed in MIL-M-38510D or MIL-STD-883.

16. SUGGESTIONS FOR MIL-STD-883

This study revealed that to obtain repeatable and accurate data, certain precautions are required during test. In order to ensure that these precautions are taken, certain changes and additions to MIL-STD-883 are suggested.

As was previously discussed, I_{OS} measurements are affected if more than one output is shorted at a time, a practice that can cause power dissipation greater than the absolute maximum rating of the DUT. This practice is contrary to several general precautions in both MIL-STD-883 and MIL-M-38510 slash sheets. However, these general precautions are secondary test requirements. Therefore, the restriction is not always obvious to test engineers. This problem can be eliminated if paragraph 3 of Method 3011.1 is revised to read as follows:

> The device shall be stabilized at the specified test temperature. Each output per package shall be tested individually. Output terminals not under test shall be open. Output terminals shall not be forced to the test condition voltage potential for a period longer than 5 seconds.

Differently defined temperature ambients were found to result in different junction temperatures for the same ambient or case temperature. MIL-STD-883B, paragraph 4.5.8 states

> Control of junction temperature. Where the application of the specified electrical inputs during test will cause the device or any internal junction temperature (T_J) to differ from the specified test temperature, case temperature (T_C), or ambient temperature (T_A) by more than $\pm 2^{\circ}C$, the following precautions shall be observed, as applicable: Where it is required that $T_J = T_A$ or T_C, the device shall be temperature stabilized in the power-off condition until the device temperature is within $\pm 2^{\circ}C$ of the case or ambient temperature, as applicable, and the prescribed power-on measurement shall be made as quickly as possible (and in no case in excess of 30 seconds) after the application of electrical inputs. Where it is required that T_J reach a normal operating level in excess of T_A or T_C, the device shall be stabilized for a sufficient period of time in a power-on condition with all specified electrical inputs applied to allow T_J to reach a temperature of at least 80 percent of its stable value under the specified test conditions.

As written, the requirement effectively minimizes the differences in junction temperature which can occur in testing the devices used in this study in differently defined ambients. It requires power-off until the test is started, as well as taking measurements as rapidly as possible to minimize test time. However, while these precautions are adequate for small scale devices, a large RAM will probably require test times in excess of 30 seconds. The T_J at normal operating level would be in excess of T_A and T_C in this case, but the actual T_J value would differ depending upon the temperature ambient. In order to standardize these measurements, MIL-STD-883B, par. 4.5.3 should be expanded to define a standard temperature ambient, with the manufacturer free to adjust other ambients to produce equivalent results. Since a fluorocarbon bath is not representative of a typical end-use environment, and both fluorocarbon and airstream environments lead to testing with T_J near to T_A or T_C, it is suggested that T_J at a "normal operating level" be further defined as T_J at a "normal operating level in an airstream with a flow in excess of 3 ft^3/min over the DUT."

Measurements were found to be affected by a number of parameters unique to ATE, such as pin condition settling time and the lack of an ideal ground path. In order to remove the effects of these parameters, MIL-STD-883 needs to define some parameters of an ATE environment in the same manner that it specifies accuracy in paragraph 4.3.3 or permissible temperature variation in environmental chambers in paragraph 4.3.1.

It is suggested that a paragraph be added to Test conditions to define those parameters affecting ATE test results. This paragraph should include the definition of an acceptable open condition and an acceptable ground path. An acceptable open could be defined as $\leq$50 pf and $\geq 10^{10}$ ohms and an acceptable ground path as $\leq$0.1 ohm and $\leq$200 nH.

A second item in the new paragraph should treat the problem of connecting a measurement system to an output, and then finding that the output has changed state. There should be a requirement that outputs shall be checked for proper state (proper state being defined by the type of measurement,

i.e., high level for V_{OH} and I_{OS} and low level for V_{OL}) after the establishment of all measurement conditions. If the proper state is no longer present, the device must be conditioned to induce the proper state before measurement.

17. CONCLUSIONS

This study was conducted to evaluate the electrical test conditions of the MIL-M-38510 slash sheet specification for some small and medium scale integrated circuits in an automated test environment. It was determined that ATE is capable of testing these devices to end use requirements. There are some problems inherent in ATE equipment when testing to the specification requirements as they are presently written. However, if the revisions that have been recommended in this report are incorporated, the specifications and the automated test equipment will be more compatible.

The data obtained during this study supports the following conclusions:

1. The measurement sequence of different DC parameters does not affect test data provided measurement times are short.
2. Temperature sequence does not affect test data provided that an adequate stabilization time at temperature is allowed. For the TP450A used in this study, a stabilization time of 60 seconds proved adequate.
3. The sequence of AC parametric measurements does not affect test data. However, since the specification sequence minimizes required preconditioning, specifying that these measurements be run in sequence would minimize the amount of preconditioning information that should be provided.
4. The sequence of measurements of the same DC parameter does not affect test data but many sequences require additional preconditioning. The order in which V_{OH}, V_{OL}, and I_{OS} measurements are taken on such sequential devices as flip-flops, counters, and shift registers should be specified.
5. Differently defined ambients result in different junction temperatures while testing at a specified T_A or T_C. Testing in fluorocarbon maintained T_J closest to T_A. Testing in an air stream produced junction temperatures approximating those of testing in fluorocarbon. Testing in still air or at case temperature in still air produced results similar to fluorocarbon when test times were short, but produced data indicating higher junction temperatures when test times were lengthened. A modification to MIL-STD-883 is proposed to assure that test results are not dependent on temperature environment.
6. Some variable measurement conditions should be more fully specified. Specifying V_{IL}, V_{IH}, and PRR for truth table testing would improve the consistency of the measurements and provide V_{IL} and V_{IH} data that cannot be obtained from other measurements in the specification.

7. Pin condition settling time was found to affect DC parametric data. Schottky and low-power Schottky devices exhibited leakage currents which rose with increasing pin condition settling time. CMOS V_{ICP} measurements required pin condition settling times in excess of 20 milliseconds. In addition, the pin application sequence study indicated that attaching the measurement system of ATE to the output of the DUT can result in the DUT changing state and yielding a false measurement. To obtain consistent and repeatable data, a modification to MIL-STD-883 is required to deal with these problems which are peculiar to automated test equipment.

8. AC parametric data did not change for the devices tested for input waveform rise and fall times of 4 and 10 nanoseconds. It is concluded that specifying t_r and t_f as $\leqq 10$ nanoseconds would be acceptable from the standpoint of device performance and would permit a wider range of ATE to test to the specification.

9. The pin application sequence study revealed that in DC parametric testing, DC conditions must be established before the pulsed inputs are applied. This is necessary to ensure that the desired device state is obtained.

10. The sequence of time measurements does not affect the data, provided that the necessary preconditioning is performed. Additional preconditioning information is required in the MIL-M-38510 slash sheet specifications.

11. Undesignated prior output states were found to affect t_{PHL} for the 54164 and 54LS295 shift registers. Specifying the prior output states is required.

12. Improper loading of outputs other than the output under test affects I_{OS} measurements. An addition to MIL-STD-883, method 3011 is proposed to remove this effect.

13. Open and ground conditions in an ATE environment are less than ideal. Acceptable conditions must be defined. Conditions of open ≤ 50 pF, $\geq 10^{10}$ ohm and ground ≤ 200 nH, ≤ 0.1 ohm are proposed. The proposed values are a compromise reflecting the capabilities of ATE. They also assure acceptable device performance in application.

Other conclusions drawn from this effort include the following:

1. Currently specified tri-state measurements can be implemented only with great difficulty on current ATE. An alternative technique is presented, but the need for further study is indicated.

2. Currently specified f_{MAX} tests cannot be implemented on many automated testing systems because of high PRR requirements. One alternative evaluated was found to be acceptable for most applications.

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